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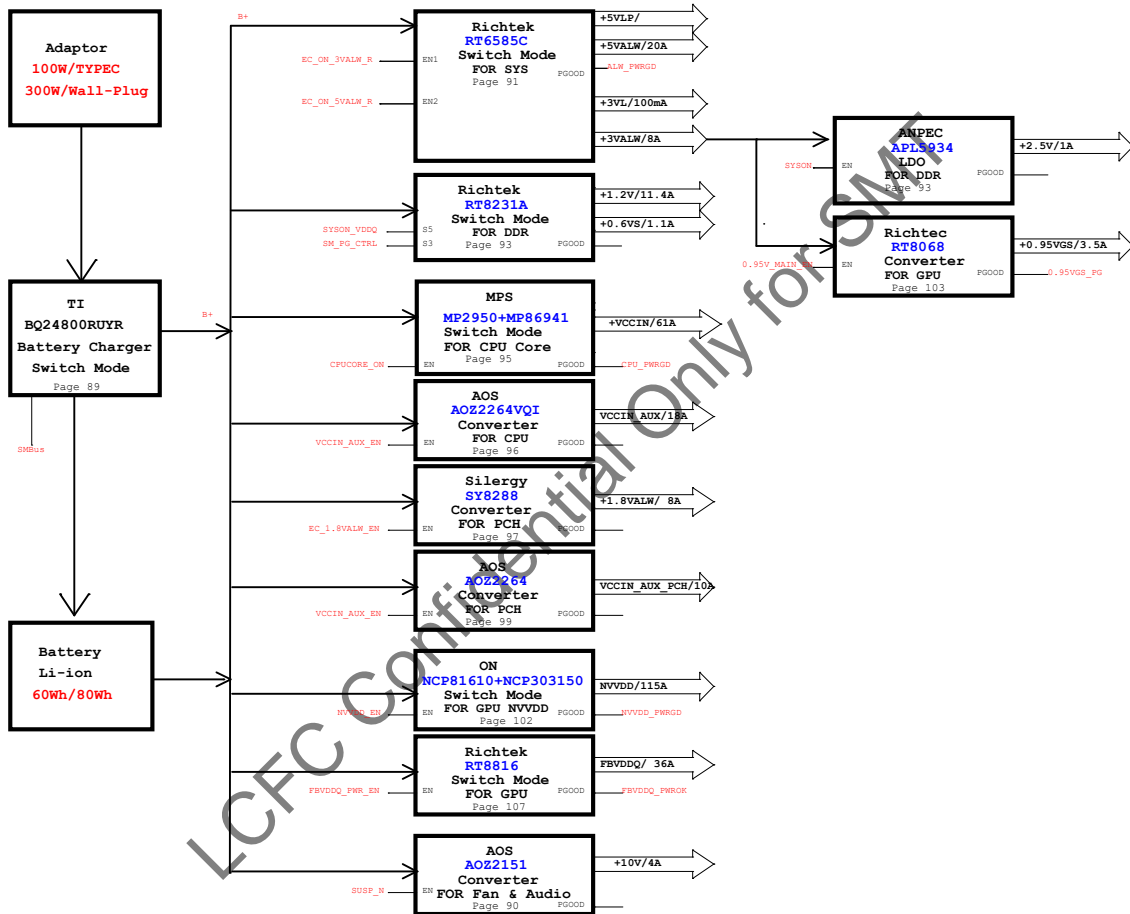
Yx70 GN20E M/B Schematics Document

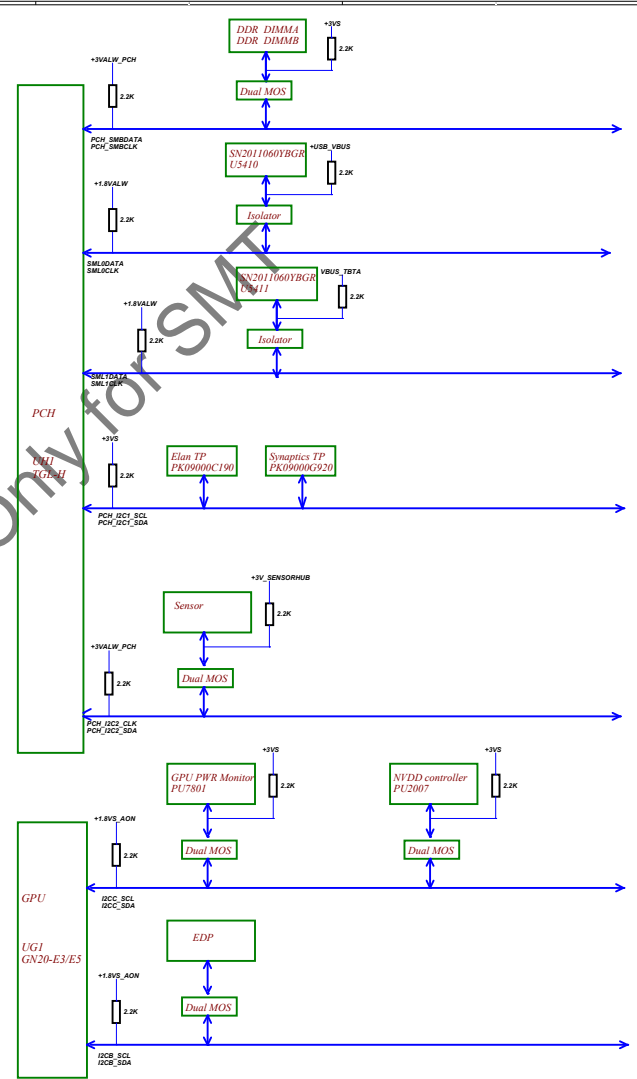
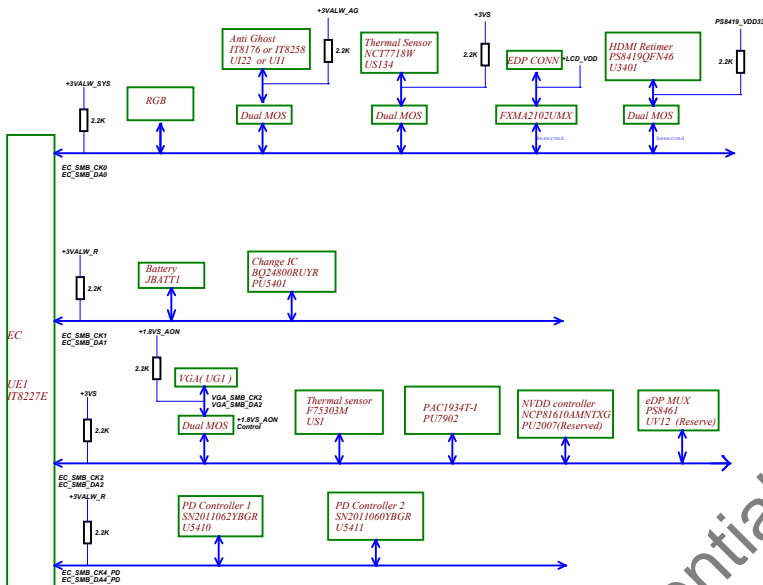
Alder Lake P-Processor with DDR5 + NV GN20-E GPU

2021-11-29

REV: A0

Security Classification	LC Future Center Secret Data		Title		
Issued Date	2018/08/02	Deciphered Date	2018/08/02		Cover Page
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SMBUS Control Table

Device	Address	Read	Write	Control	Power	Temp	Light	Audio	Video	Other
EC SMB D01	0x0000	X	X	X	X	X	X	X	X	X
EC SMB D02	0x0001	X	X	X	X	X	X	X	X	X
EC SMB D03	0x0002	X	X	X	X	X	X	X	X	X
EC SMB D04	0x0003	X	X	X	X	X	X	X	X	X
EC SMB D05	0x0004	X	X	X	X	X	X	X	X	X
EC SMB D06	0x0005	X	X	X	X	X	X	X	X	X
EC SMB D07	0x0006	X	X	X	X	X	X	X	X	X
EC SMB D08	0x0007	X	X	X	X	X	X	X	X	X
EC SMB D09	0x0008	X	X	X	X	X	X	X	X	X
EC SMB D10	0x0009	X	X	X	X	X	X	X	X	X
EC SMB D11	0x000A	X	X	X	X	X	X	X	X	X
EC SMB D12	0x000B	X	X	X	X	X	X	X	X	X
EC SMB D13	0x000C	X	X	X	X	X	X	X	X	X
EC SMB D14	0x000D	X	X	X	X	X	X	X	X	X
EC SMB D15	0x000E	X	X	X	X	X	X	X	X	X
EC SMB D16	0x000F	X	X	X	X	X	X	X	X	X
EC SMB D17	0x0010	X	X	X	X	X	X	X	X	X
EC SMB D18	0x0011	X	X	X	X	X	X	X	X	X
EC SMB D19	0x0012	X	X	X	X	X	X	X	X	X
EC SMB D20	0x0013	X	X	X	X	X	X	X	X	X
EC SMB D21	0x0014	X	X	X	X	X	X	X	X	X
EC SMB D22	0x0015	X	X	X	X	X	X	X	X	X
EC SMB D23	0x0016	X	X	X	X	X	X	X	X	X
EC SMB D24	0x0017	X	X	X	X	X	X	X	X	X
EC SMB D25	0x0018	X	X	X	X	X	X	X	X	X
EC SMB D26	0x0019	X	X	X	X	X	X	X	X	X
EC SMB D27	0x001A	X	X	X	X	X	X	X	X	X
EC SMB D28	0x001B	X	X	X	X	X	X	X	X	X
EC SMB D29	0x001C	X	X	X	X	X	X	X	X	X
EC SMB D30	0x001D	X	X	X	X	X	X	X	X	X
EC SMB D31	0x001E	X	X	X	X	X	X	X	X	X
EC SMB D32	0x001F	X	X	X	X	X	X	X	X	X

GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 --MSVDD_EN	GPIO4_GC6_MSVDD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	IGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED			
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE N18P-G61-A Control FP_FUSE	Connect to WP pin of the GPU EEPROM	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD) RSVD
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)
GPIO28	OUT	MSVDD_PWM_VID	PWM Ooutput to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVVDD_EN	NVVDD Enable RSVD	GPIO29_NVVDD_EN	(100K PU) RSVD
GPIO30	OUT	MSVDD_PSI*	Phase Shedding	UNUSED	

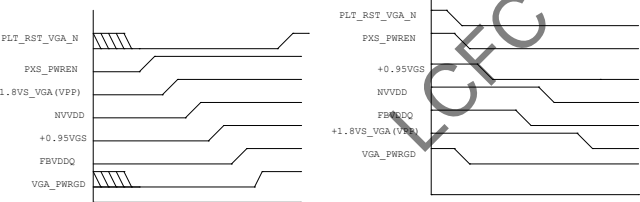
H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z803258C-HC14
L	L	H	1 (0x0001)	Micron MT61H256M32JE-14-A
L	H	L	2 (0x0002)	Hylix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung (or E7) K4ZAF3258M-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLE Reserved, do not configure

GN20x-E Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
 2. It is recommended that the delay from VFP on to FBVDDQ/GPU_POWD assertion not exceed 3ms.
 3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
 4. Power up NVVDD must be 90% before FBVDDQ can ramp-up.
 5. Refer to the JEDEC Memory SPBC for memory-related power sequencing.
 7. FBVDDQ/G, USB_VDDP and VFP_AON don't need power cycle for GC6
1. For GDDR6, VFP must be equal to or higher than FBVDDQ at all times/rise gate logic and discharge circuit as needed.
 2. All 3.3V devices that connect to the GPU must be ramp down before VFP; GPU can NOT have any 3.3V leakage path after VFP power down.
 3. Power down of FBVDDQ must be less than 10% before NVVDD can start ramp-down.

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
- 0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
- 0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
- 0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
- 0:VGA_DEVICE DISABLE

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Voltage Rails (0 -> Means ON, X -> Means OFF)

Power State	B+	+5VALLW	+5VALLW_PCH	+1.2V	Other
State					1 -> with power 2 -> power 3 -> power 4 -> power
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S3 S4/AC Only	0	0	0	X	X
S3 S4 Battery only	0	X	X	X	X
S3 S4 AC & battery don't exist	X	X	X	X	X

Power State	B+	+5VALLW	+5VALLW_PCH	+1.2V	Other
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S3 S4/AC Only	0	0	0	X	X
S3 S4 Battery only	0	X	X	X	X
S3 S4 AC & battery don't exist	X	X	X	X	X

BOM Structure Control Table

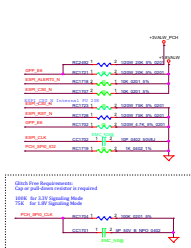
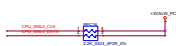
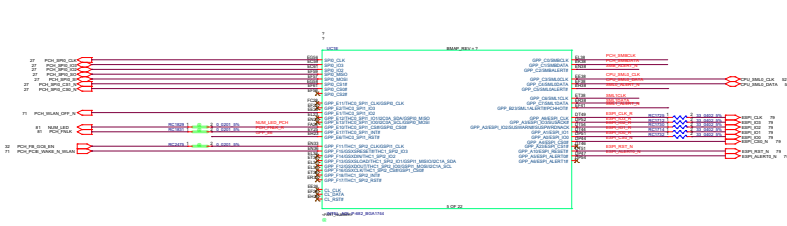
Part	Part Name	Part Value	Part Unit	Part Desc	Part Cat	Part Sub	Part Type	Part Status	Part Remark
1	100 100 100	100	100	100	100	100	100	100	100
2	100 100 100	100	100	100	100	100	100	100	100
3	100 100 100	100	100	100	100	100	100	100	100
4	100 100 100	100	100	100	100	100	100	100	100
5	100 100 100	100	100	100	100	100	100	100	100
6	100 100 100	100	100	100	100	100	100	100	100
7	100 100 100	100	100	100	100	100	100	100	100
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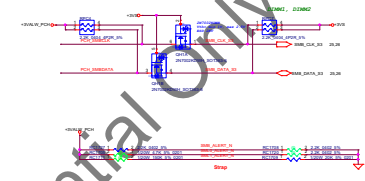
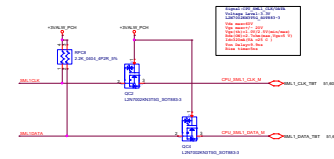
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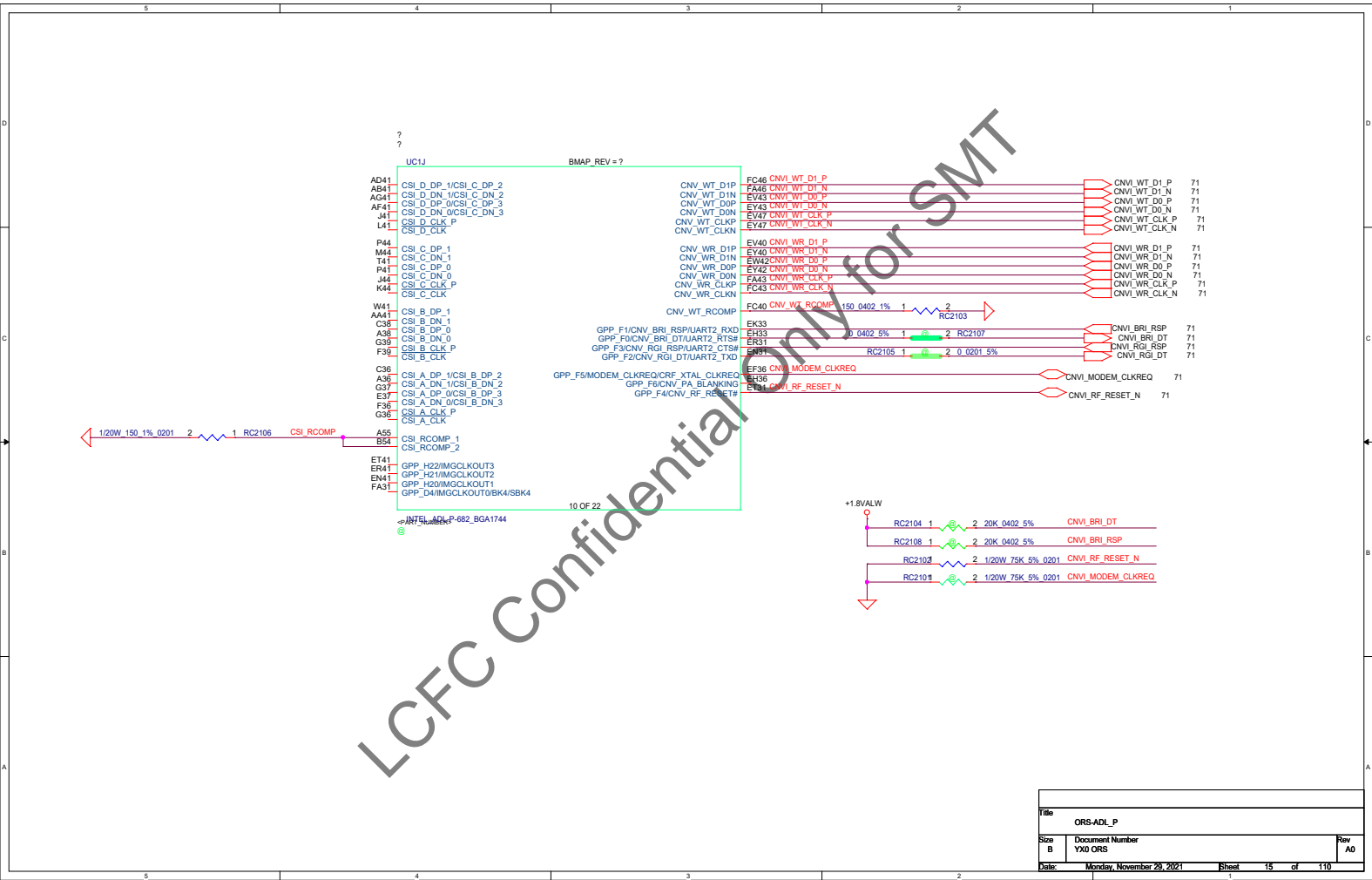


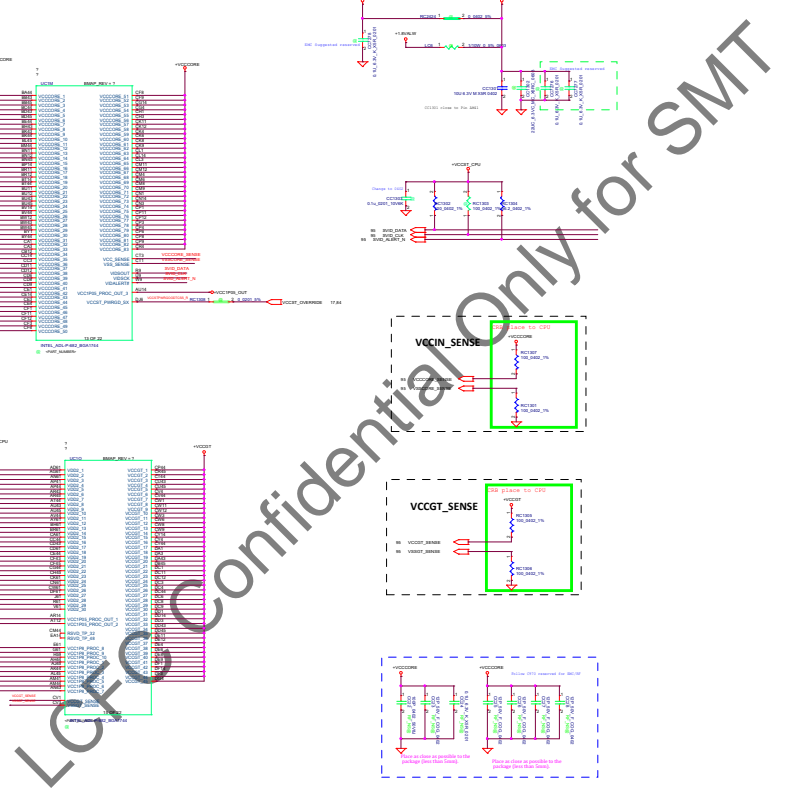
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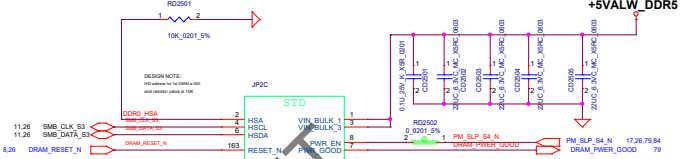
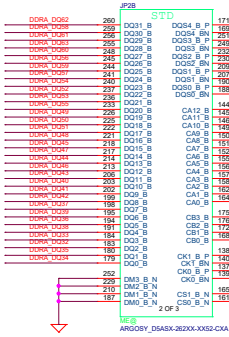
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8 DORA_DQB[63] DORA_DQB[63]

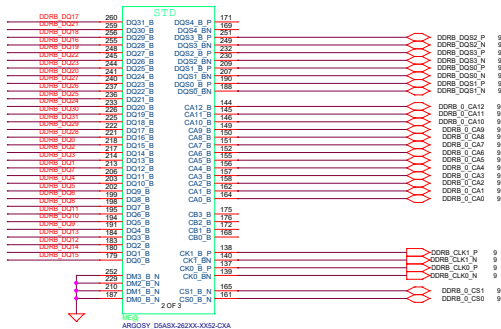


9 DDRB_DQ0_63

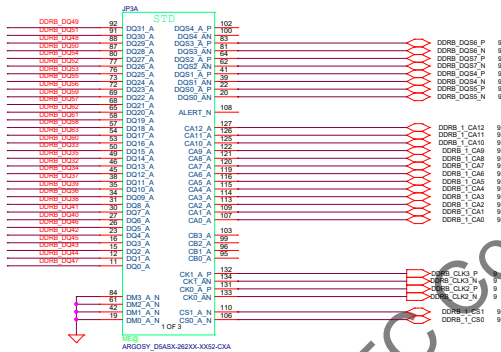
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10K 20.0K 001

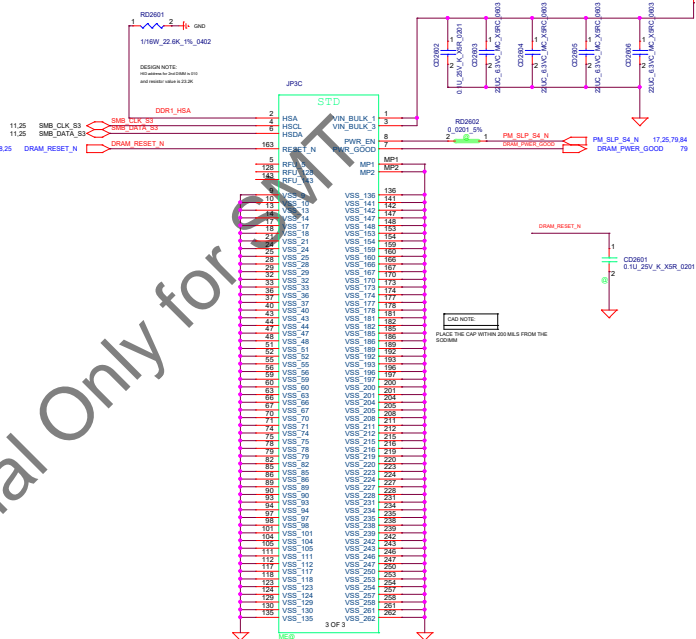


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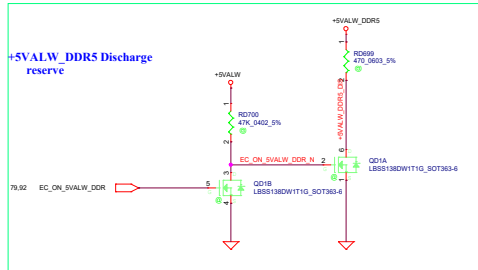



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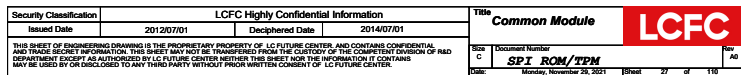
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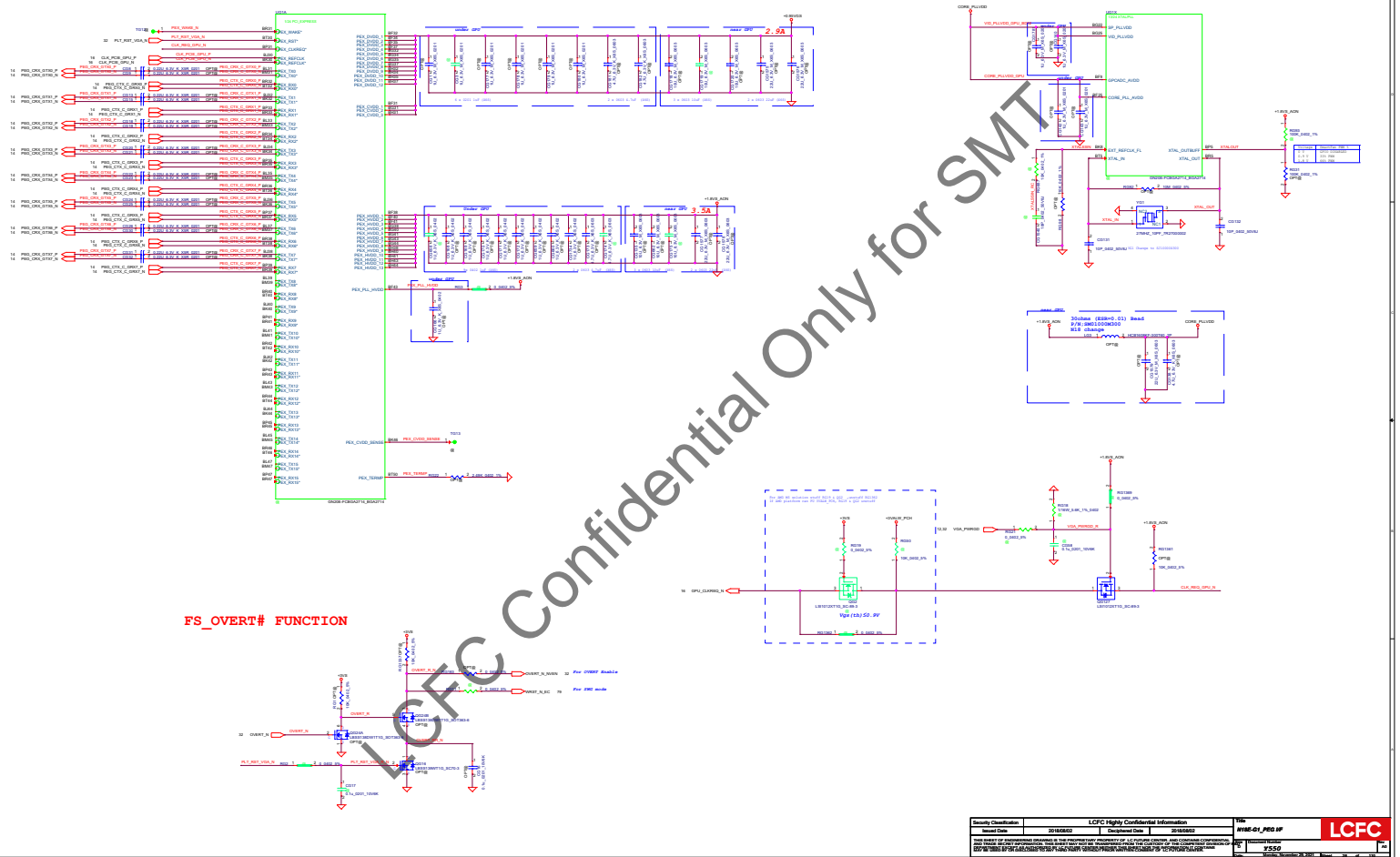


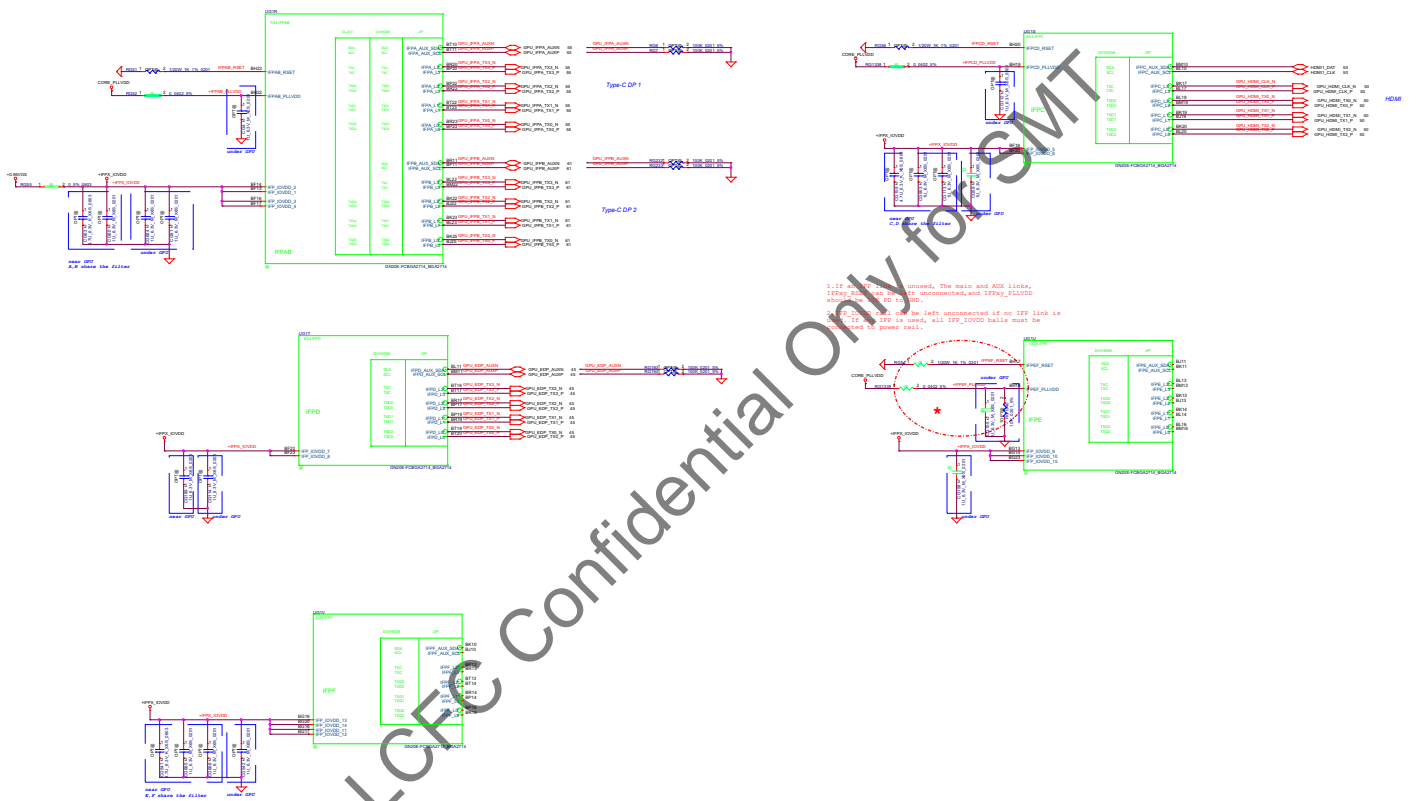
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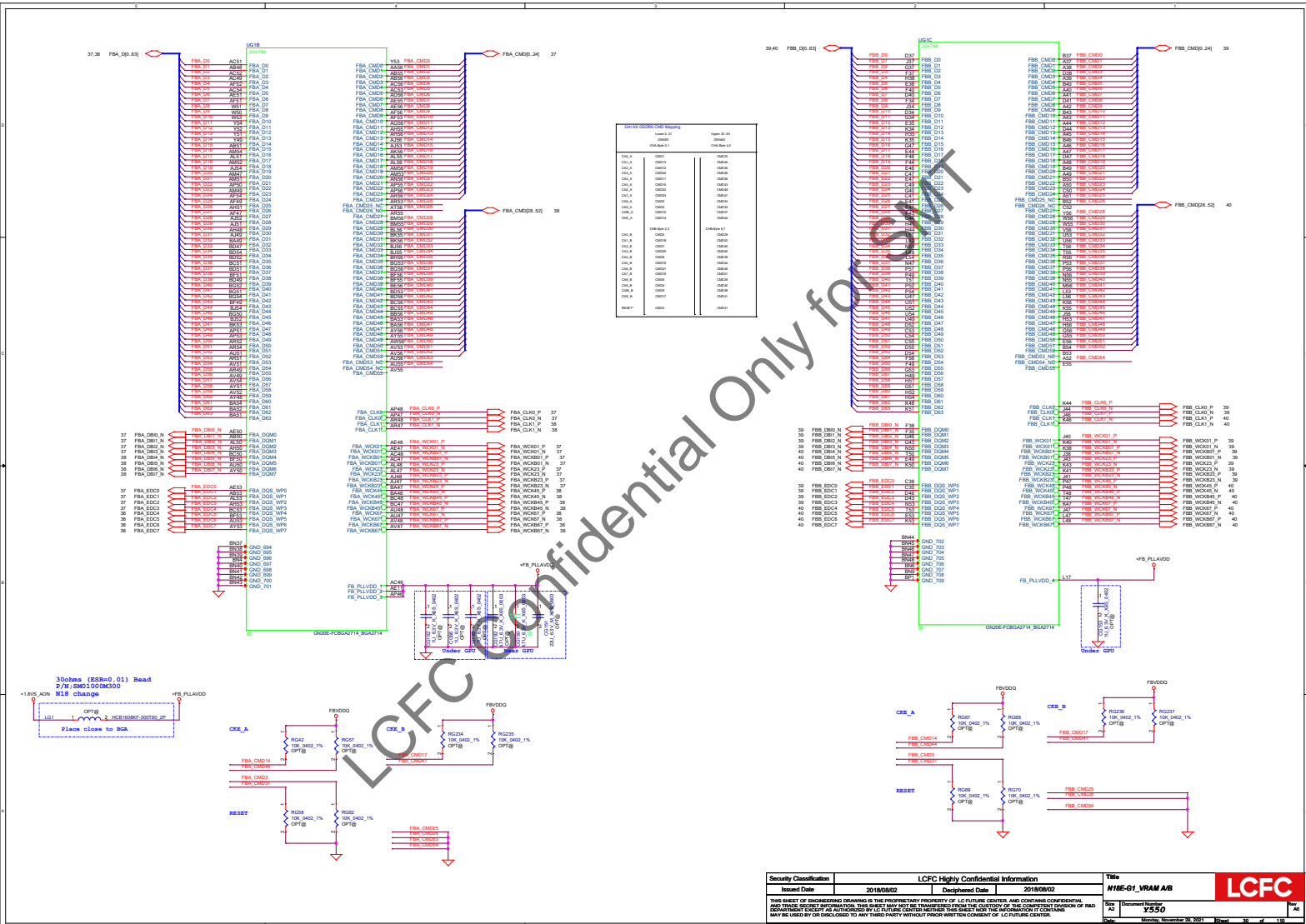


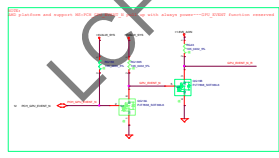
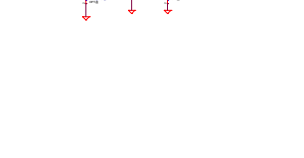
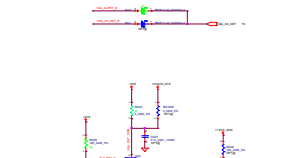
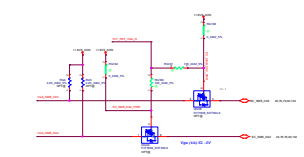
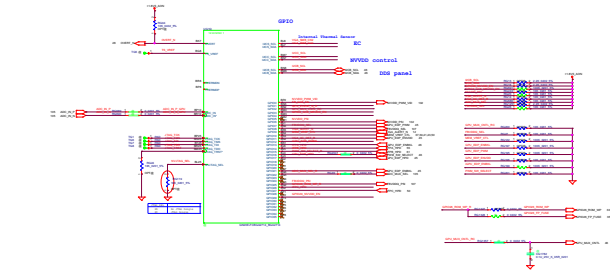
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2018/08/02				DDRVI SO-DIMM B	
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Date		Version		10	
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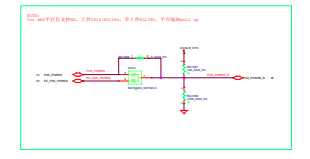
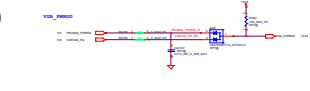
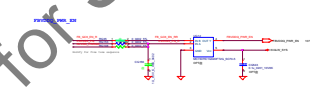
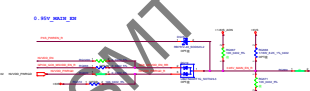




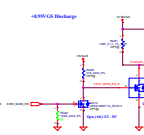
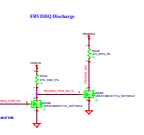
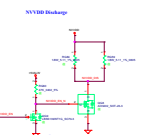


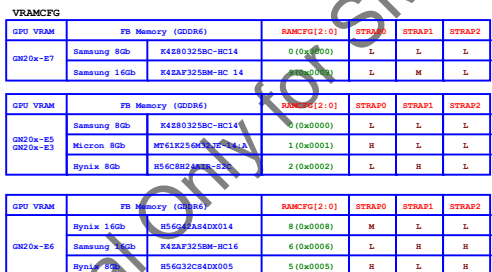
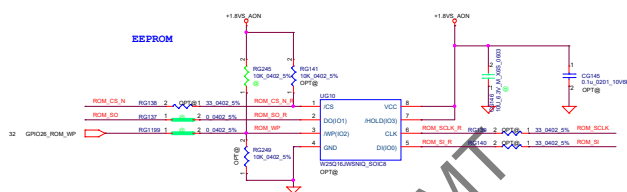


Power on/off sequence



Discharge



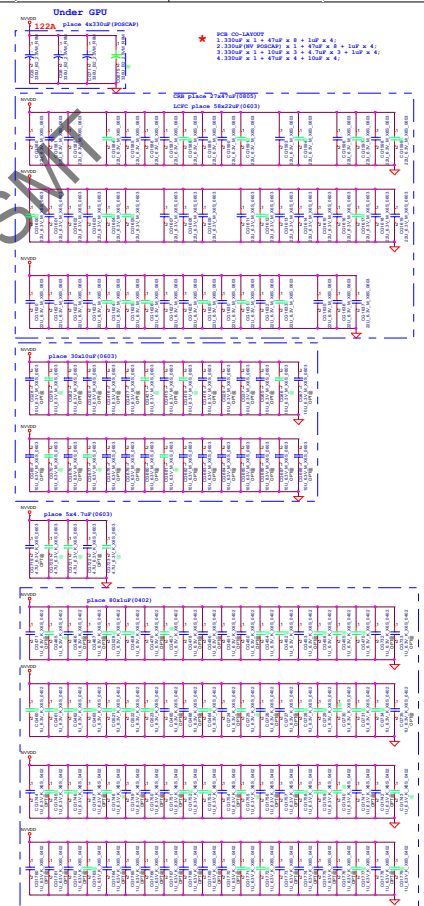
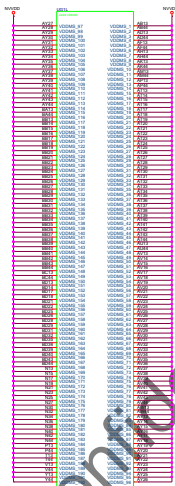
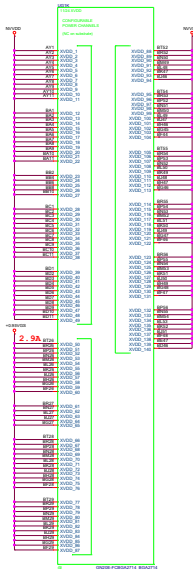
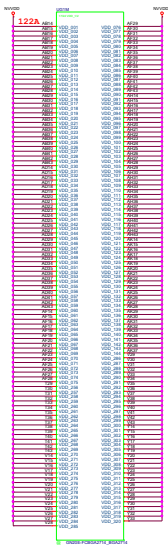


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1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

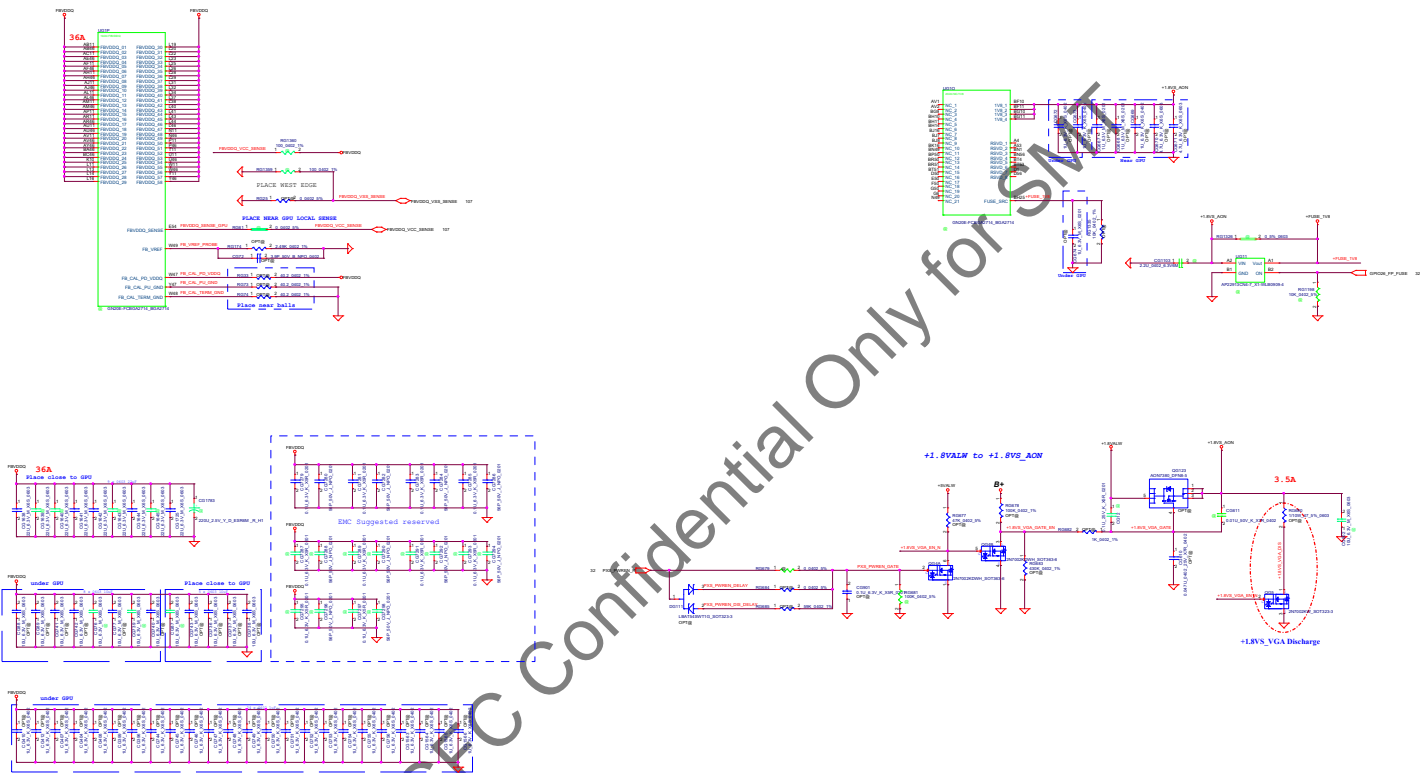
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

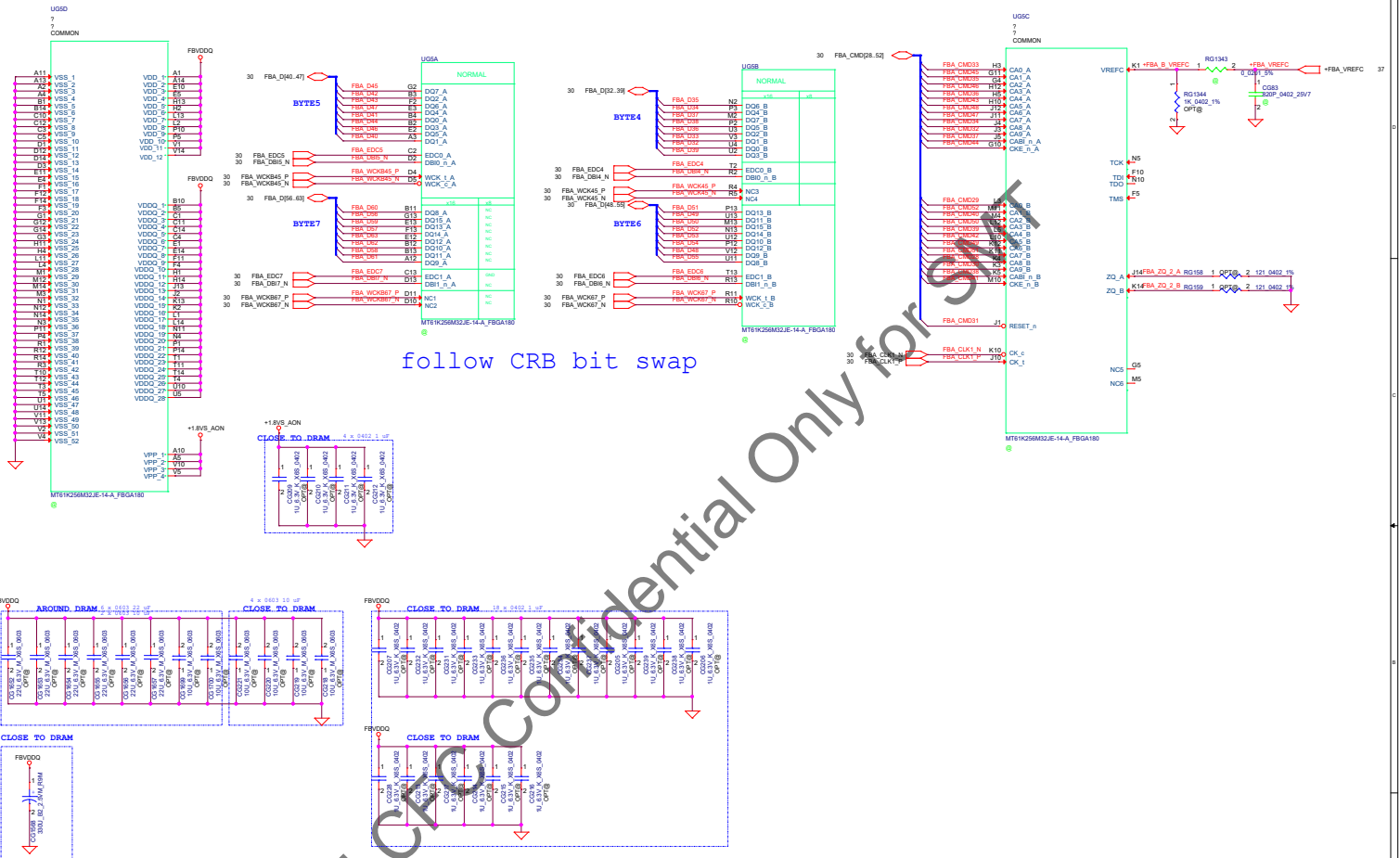
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
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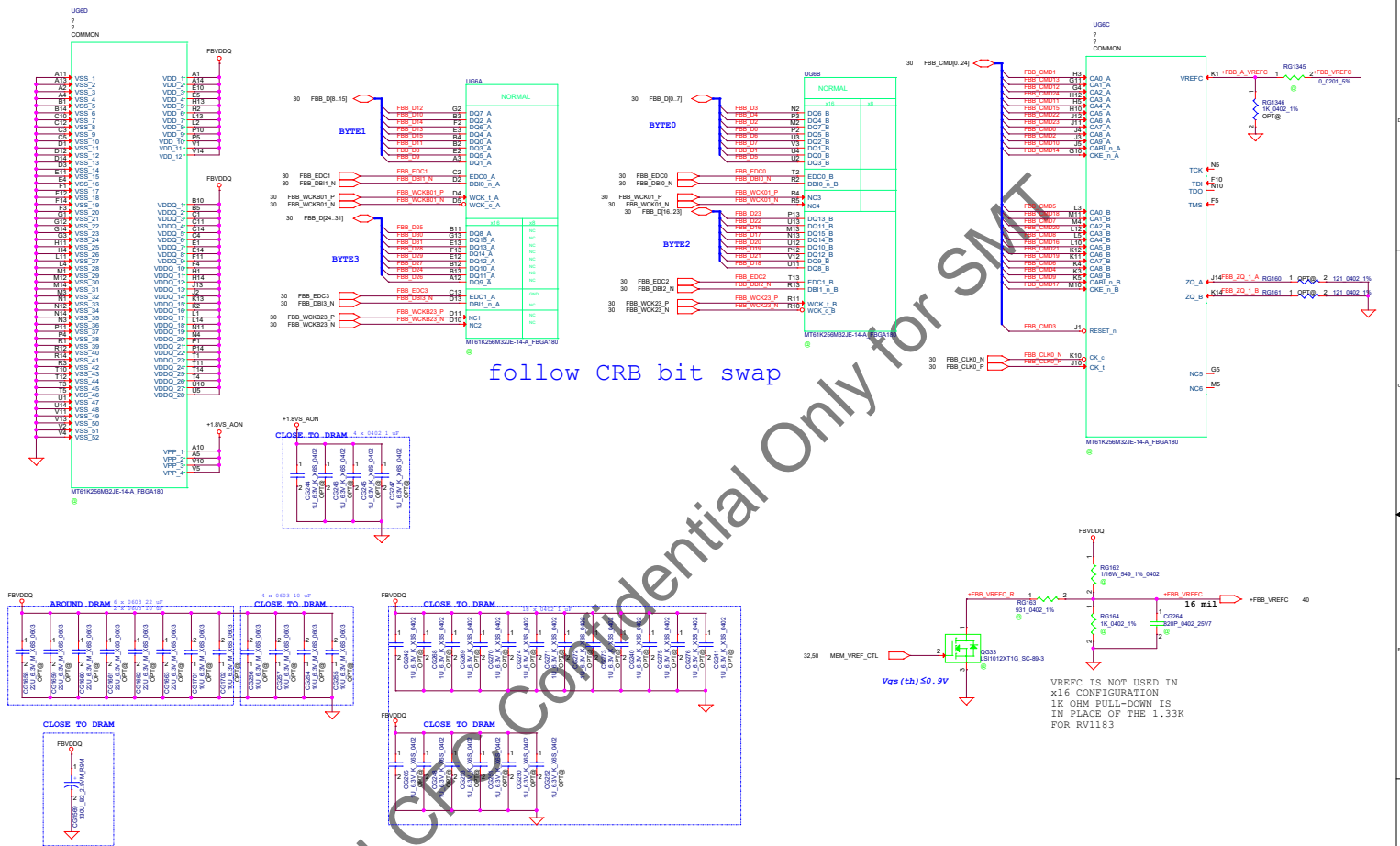


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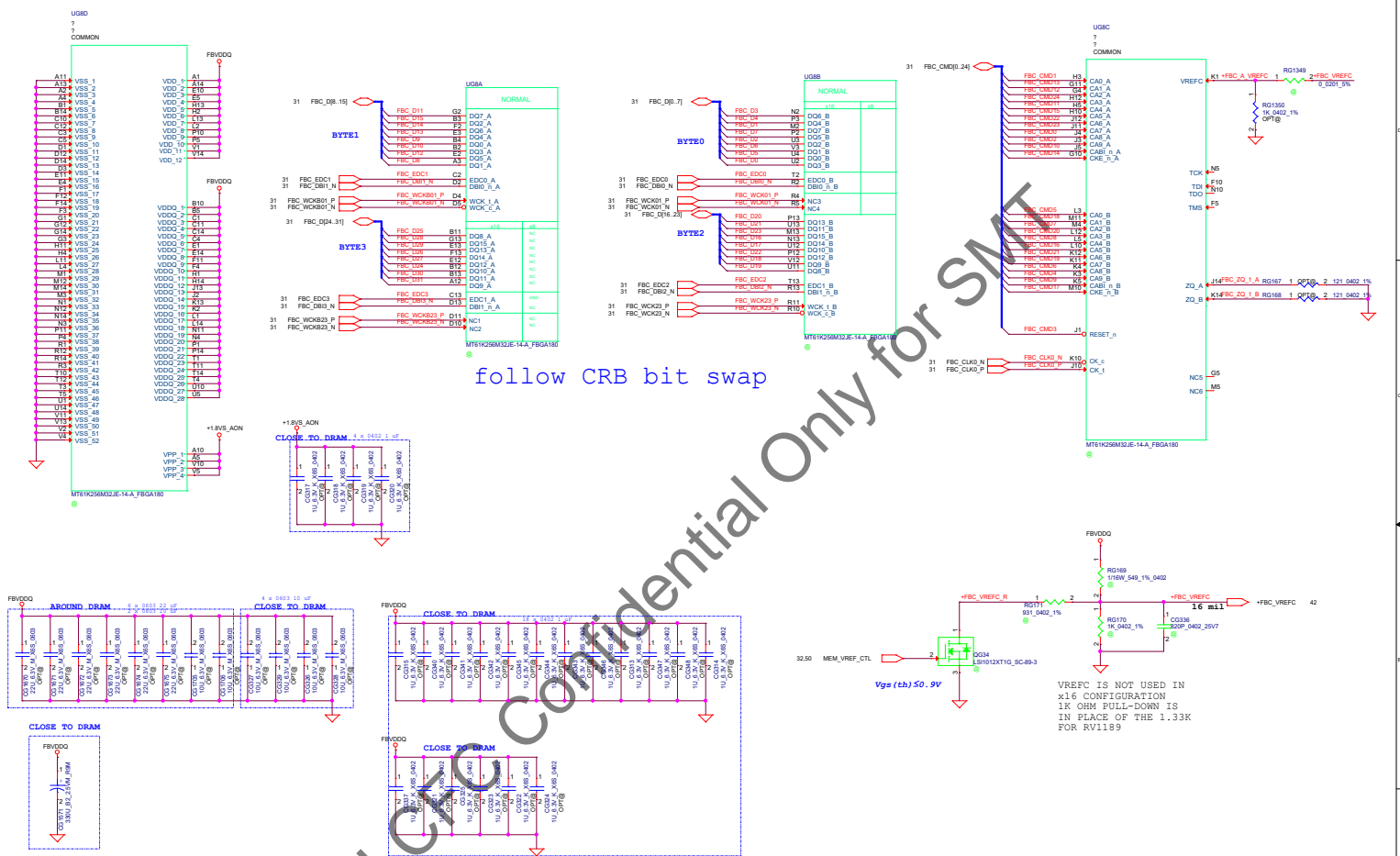


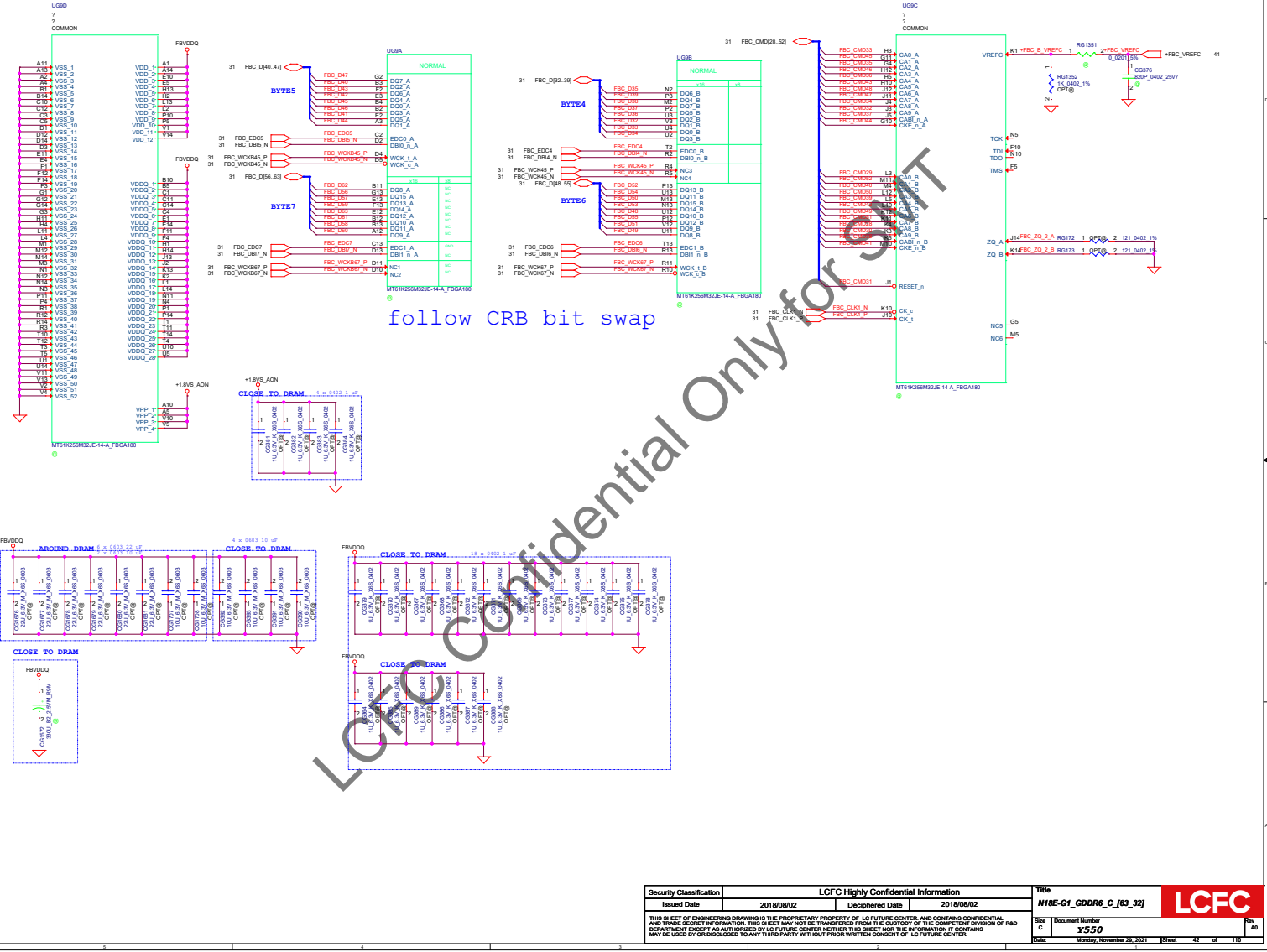


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				Rev	40
				Date	Monday, November 26, 2021
				Page	38 of 116

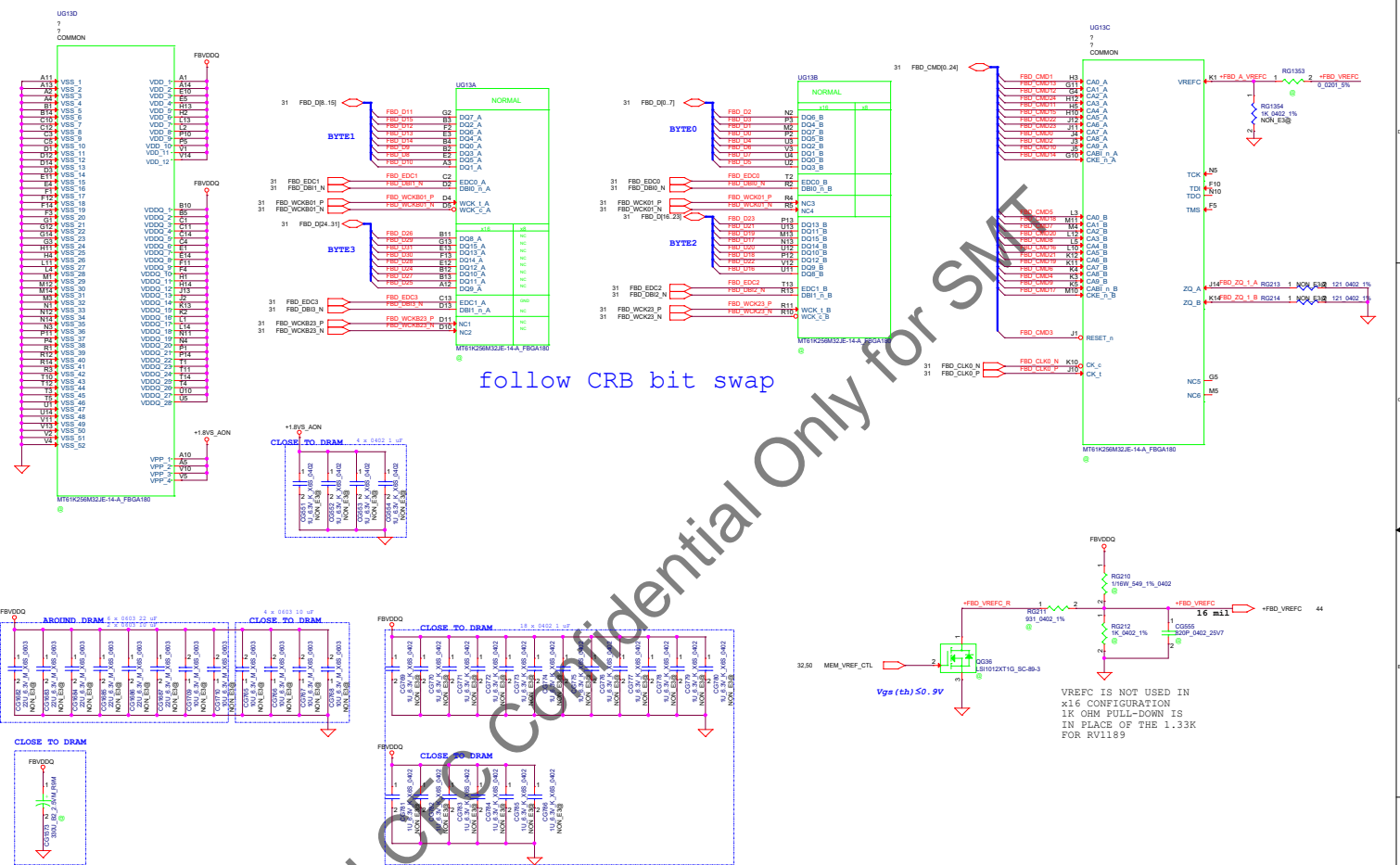


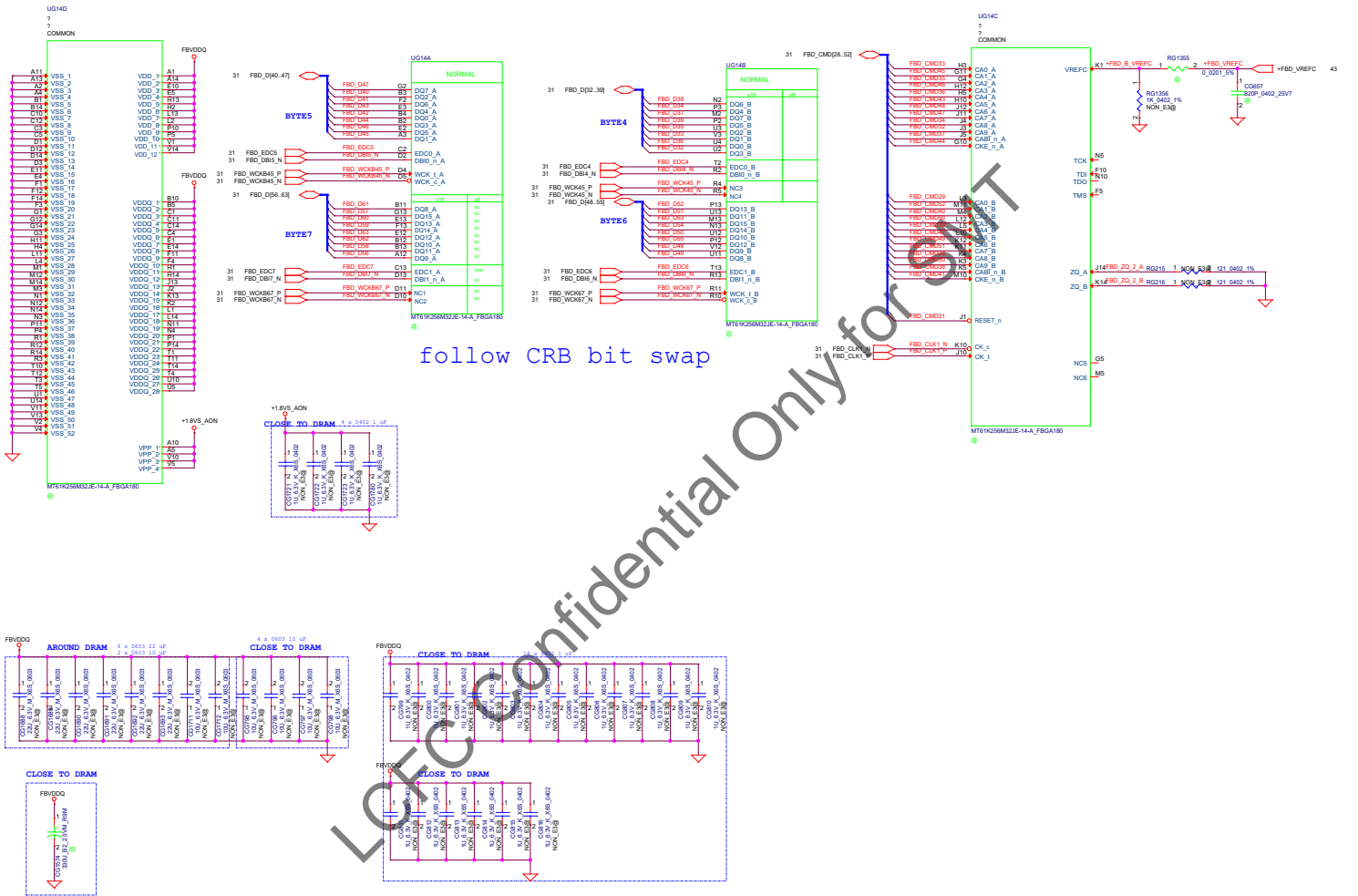
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				Rev	40
				Date	Monday, November 25, 2021
				Page	39 of 116



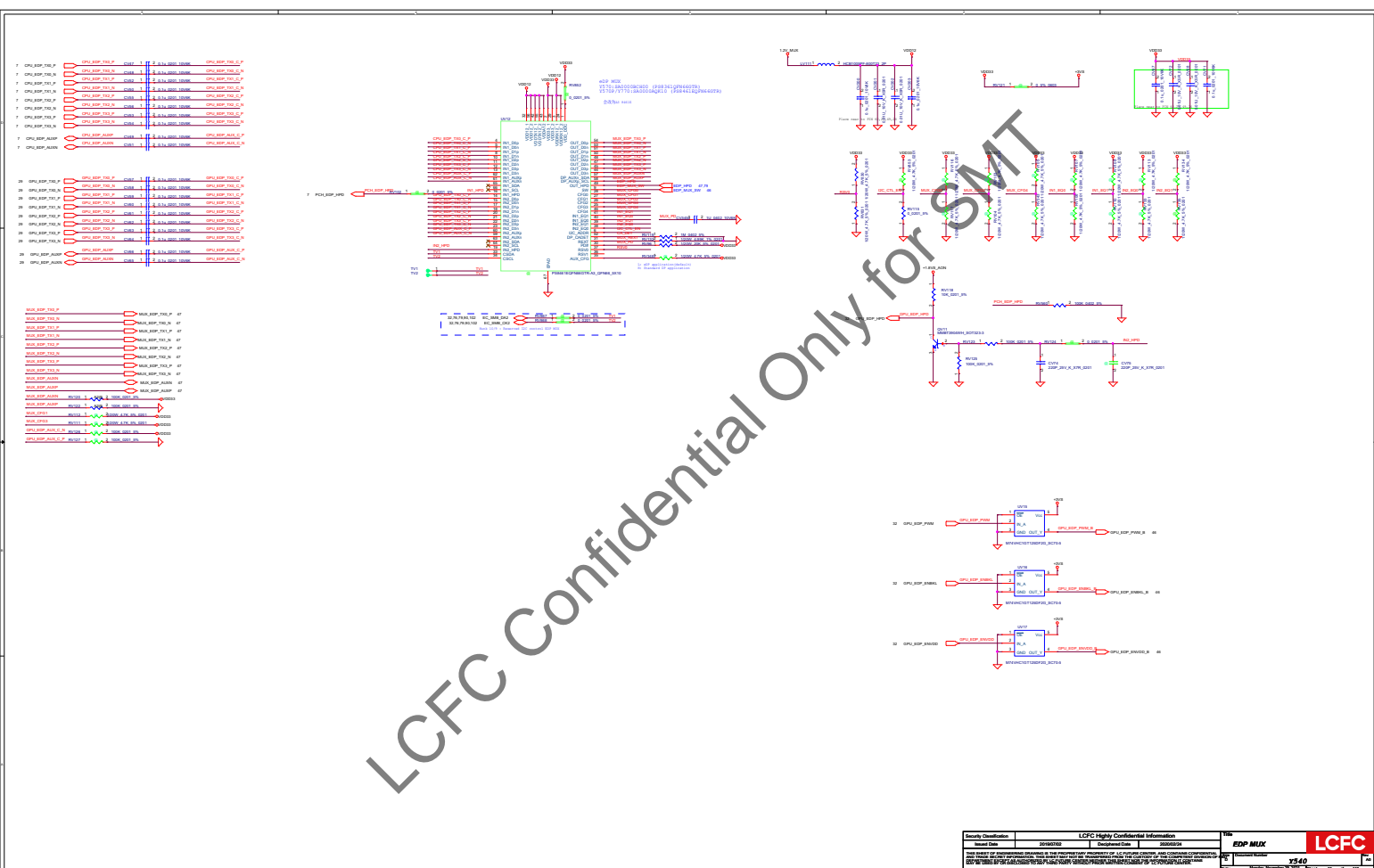


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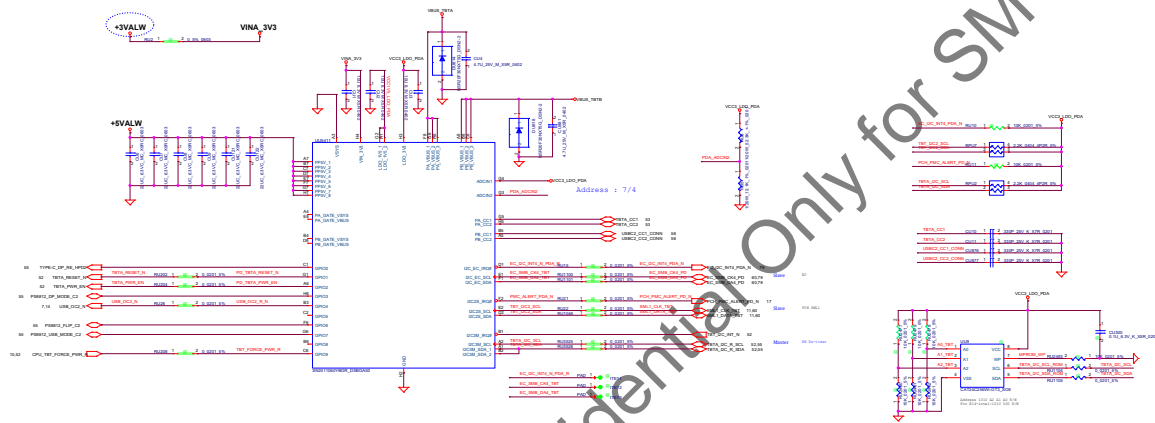
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Date:	Monday, November 29, 2021	Sheet 49 of 110

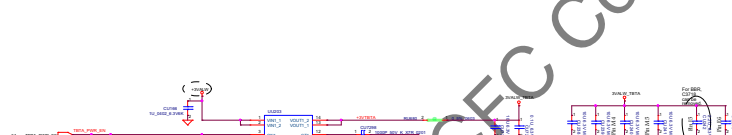
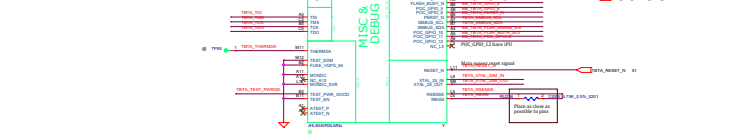
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2019/07/02		2020/02/24			

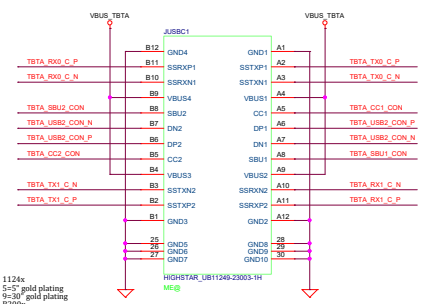
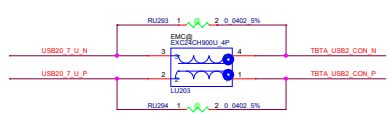
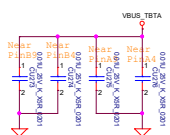
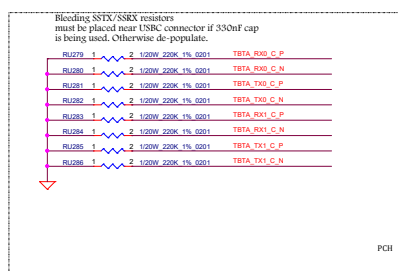
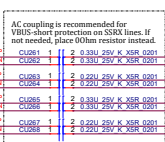
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TBT portA/rear side





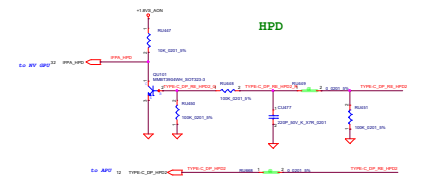
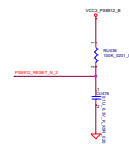
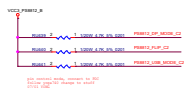
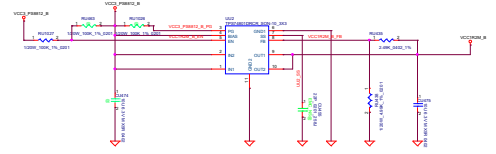
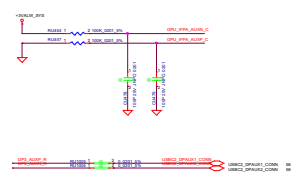
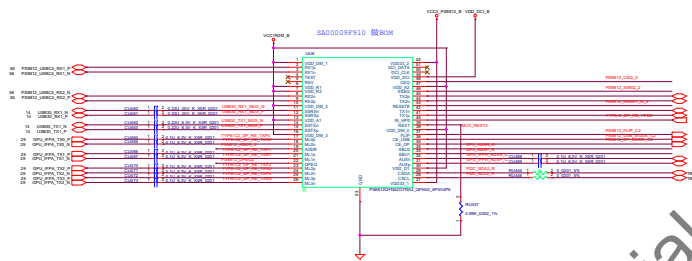
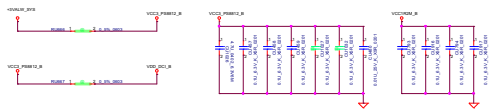


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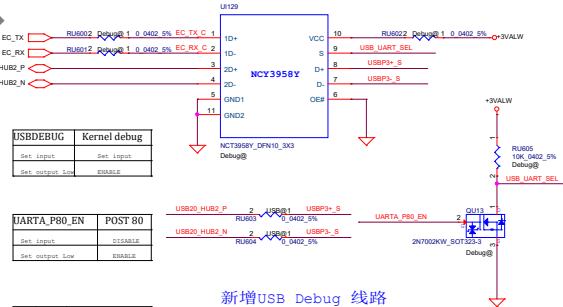
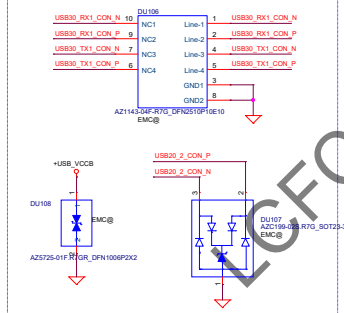
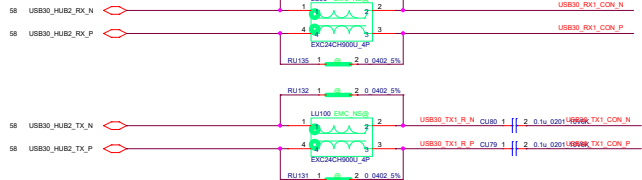
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DC V TO VS INTERFACE
LCFC
9540

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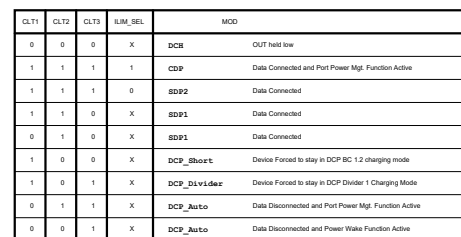
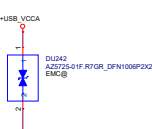


UART _m P80 _m EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)

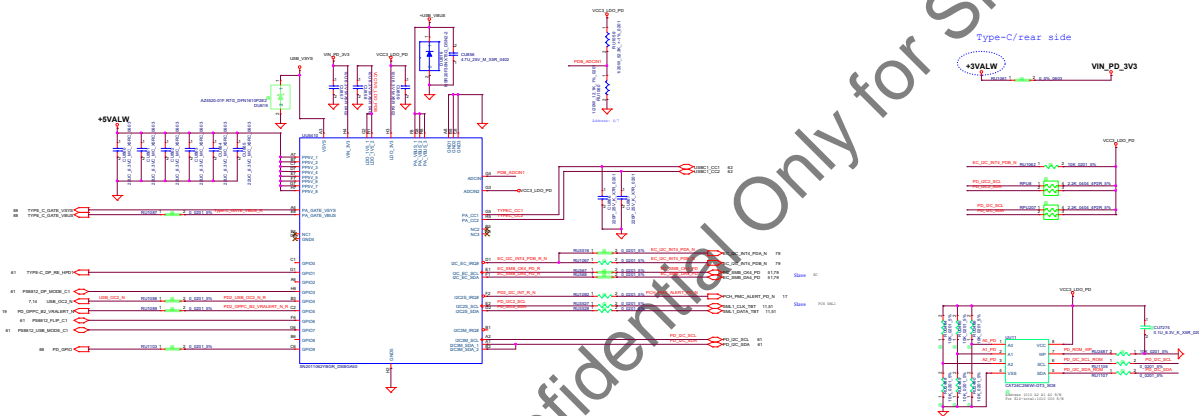
新增USB Debug 线路

[illegible]

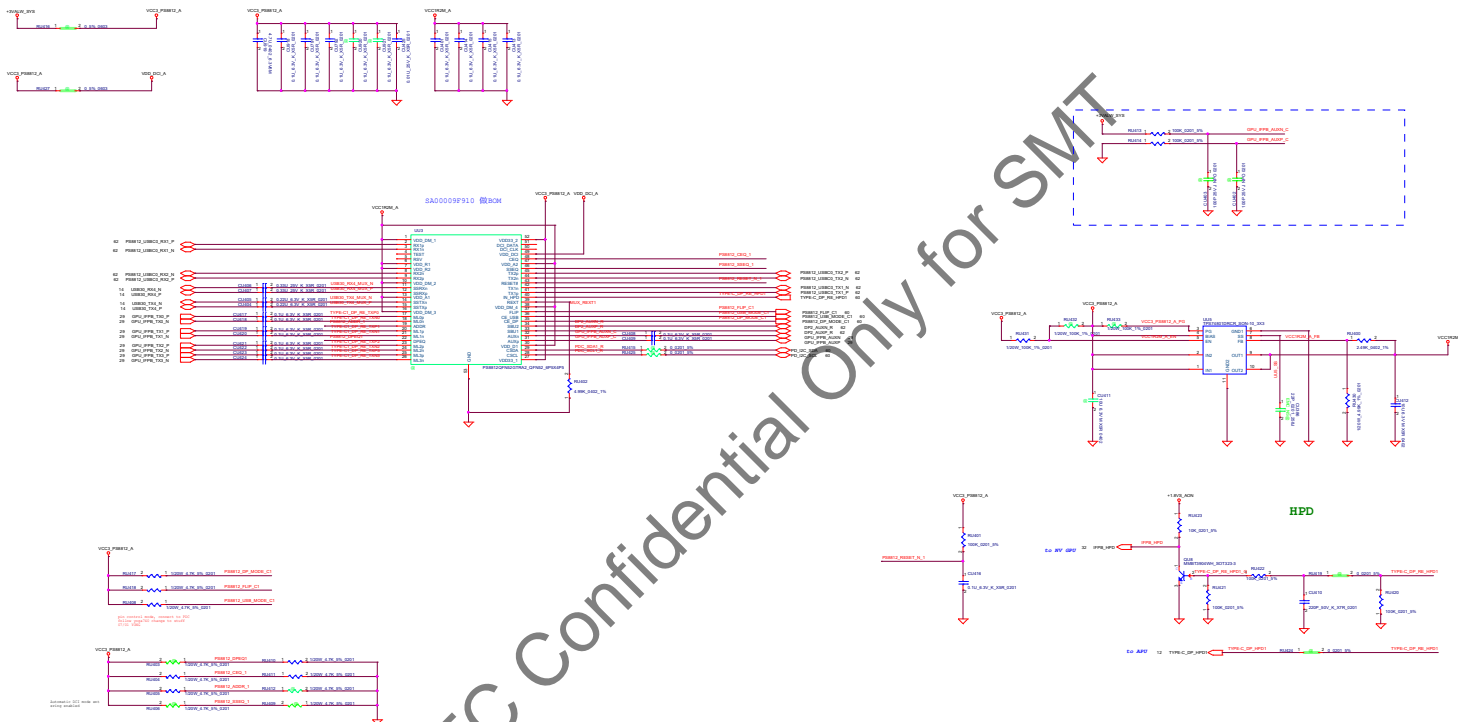


CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCR	Out held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

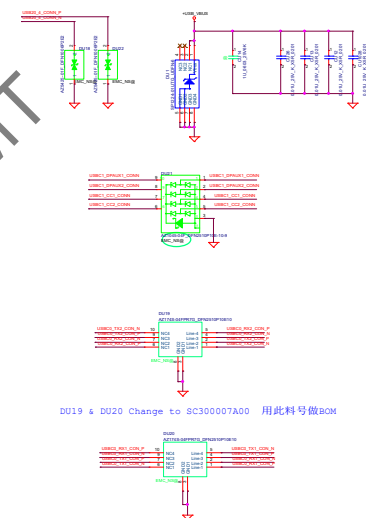
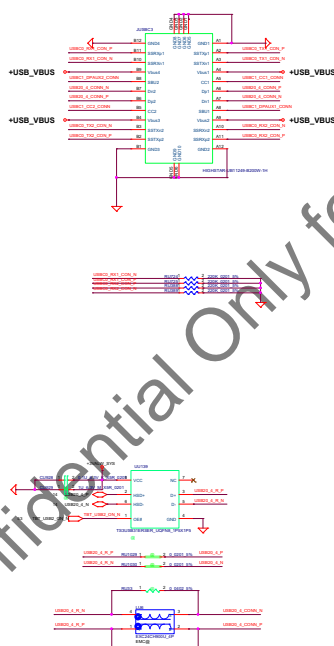
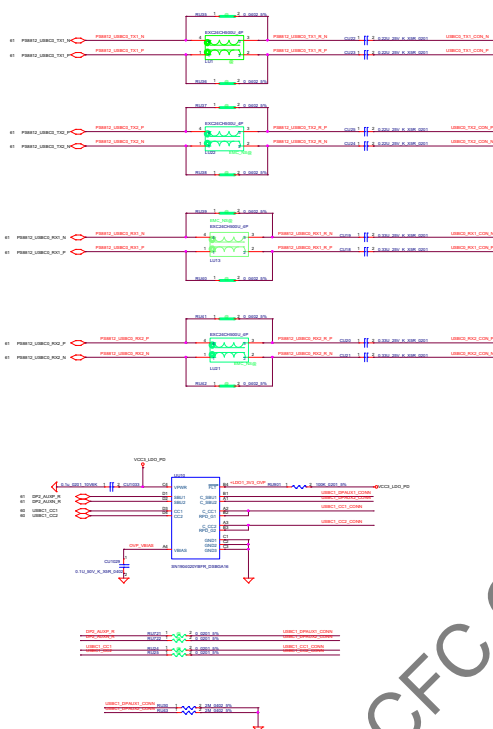
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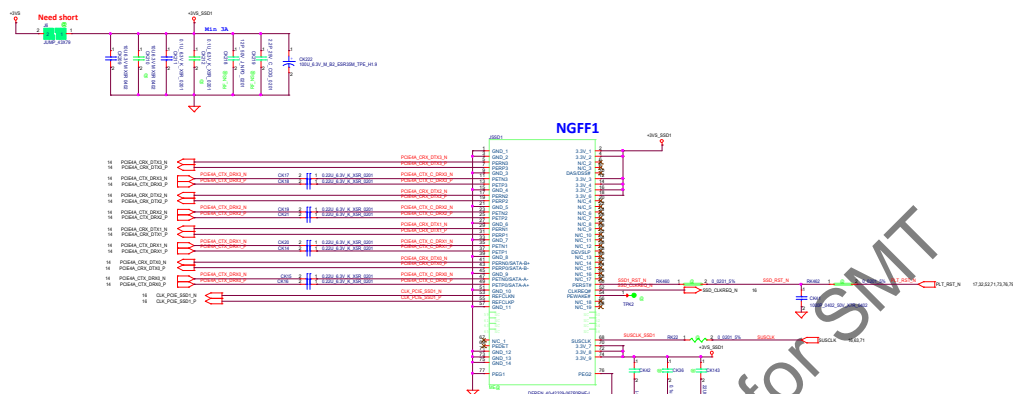


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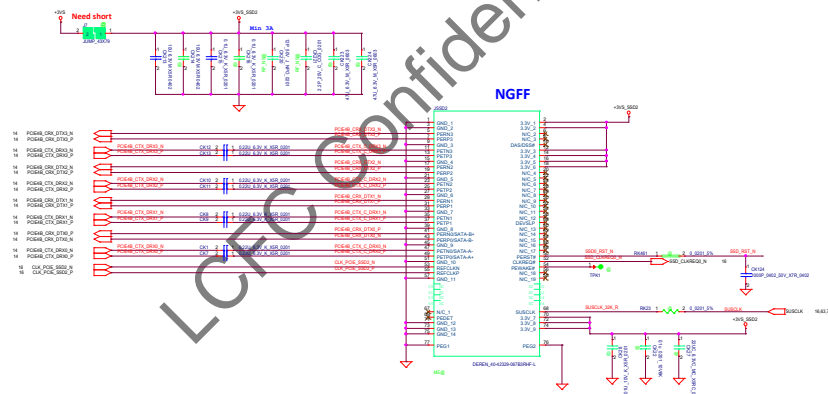


D019 & D020 Change to SC300007A00 用此料号做BCM

M.2 SSD(PCIE GEN4 from CPU)



M.2 SSD(SATA/PCIE Gen3 from PCH)



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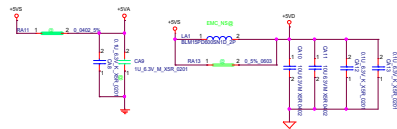
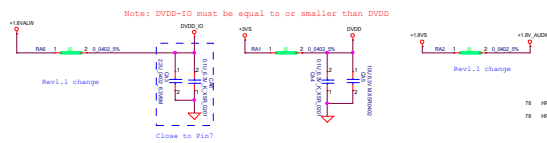
Delete USB3.0 Reapter Remove to DB board

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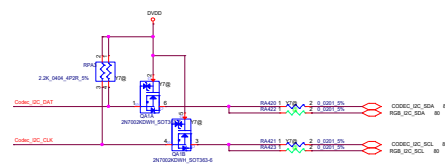
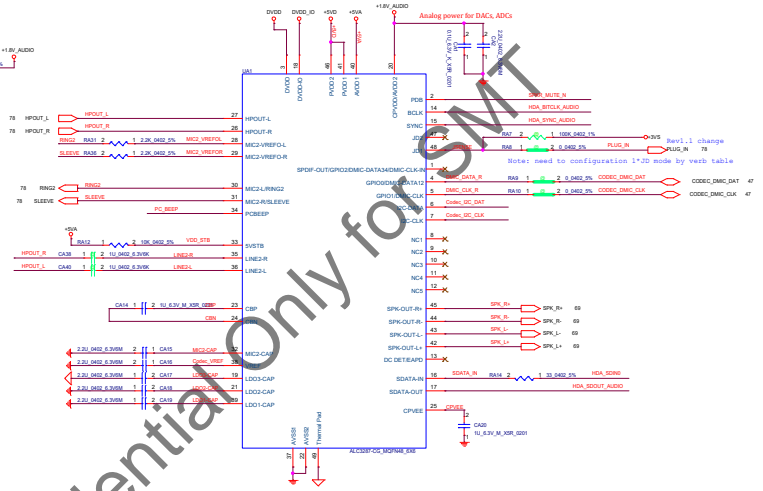
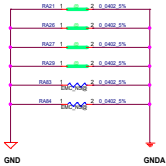
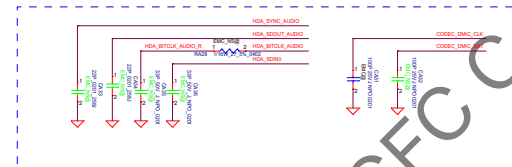
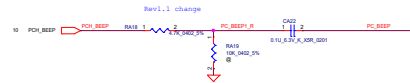
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Model Number: 28-2021		2	118	Date	Sheet #	
		1				

13 HDA_BTCLK_AUDIO
13 HDA_SYNC_AUDIO
13 HDA_SDOUP_AUDIO
13 HDA_SDRNG



Note: power beep function is removed from BIOS spec



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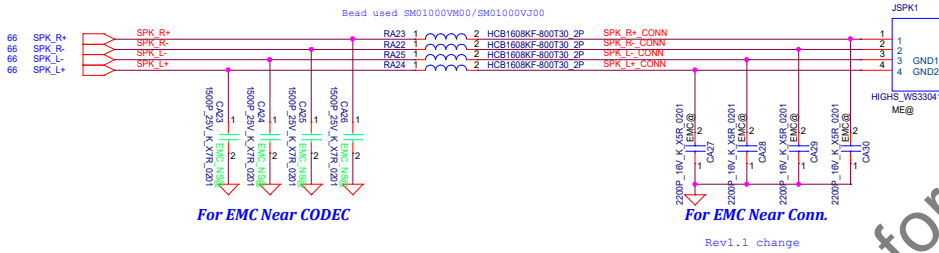
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Issued Date	2012/07/01	Deciphered Date	2014/07/01		
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Rev	C	Document Number	Audio Amplifier		Rev
Doc	Version: 00000000-00-0001		Sheet		87 of 110

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				C	Audio DSP	Rev	Rev
				Ver	Ver	Rev	Rev

Speaker

Speaker



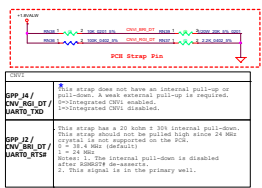
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Size	Document Number					Rev
	Audio SPK/Jack					AD
Date:	Monday, November 29, 2021					Sheet 69 of 110

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				C	Y540
				Rev	A0
Date				Monday, November 25, 2021	Sheet 70 of 115

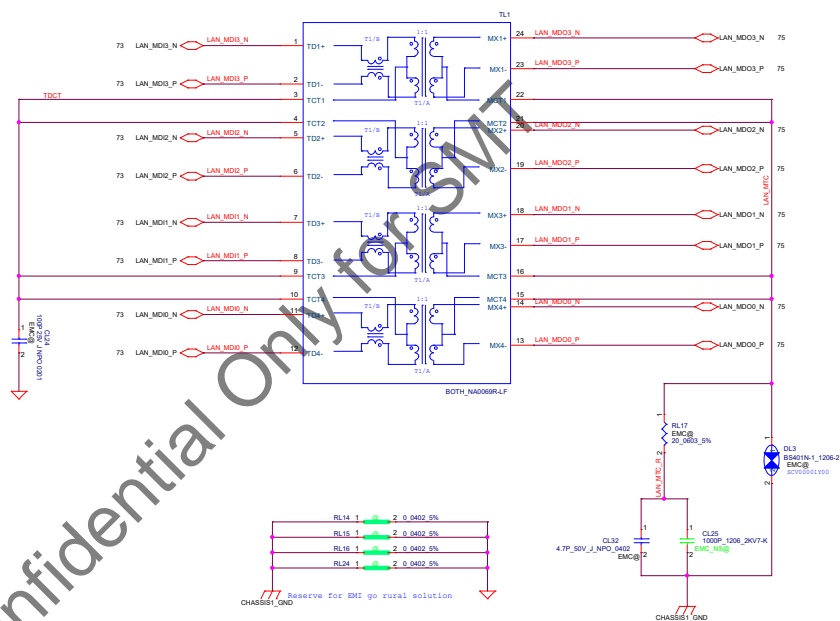
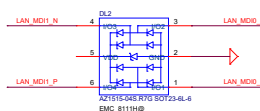
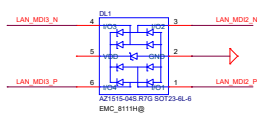
The diagram illustrates a complex PCB layout for a multi-channel ADC system. The top section shows the connection of 16 channels of an ADC12700 to a multi-channel ADC (MCD) via a 16-bit parallel bus. The bottom section shows the connection of the MCD to a multi-channel DAC (MCD) via a 16-bit parallel bus. The diagram includes various components like resistors, capacitors, and logic gates, and is labeled with component values and pin numbers. A large diagonal watermark 'LCFC Confidential Only for SMT' is overlaid on the image.




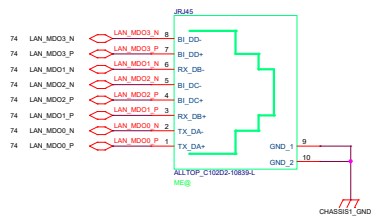
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Size	Document Number		Date	Rev
8	Reserved		Monday, November 26, 2021	A0
Sheet 72 of 110				

DL1/DL2
1'S PN:SC300005900
Place Close to TL1

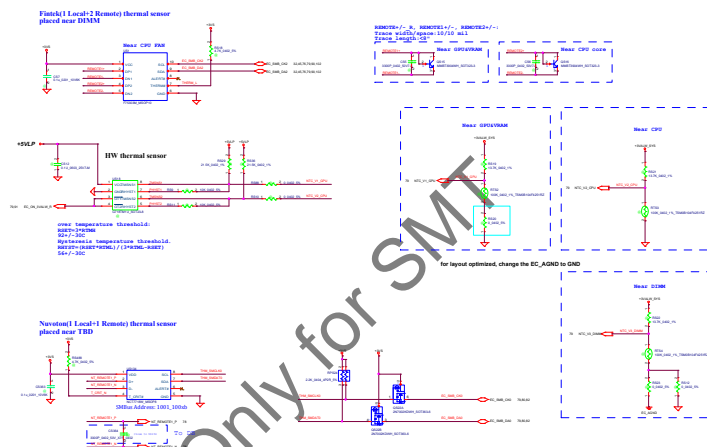
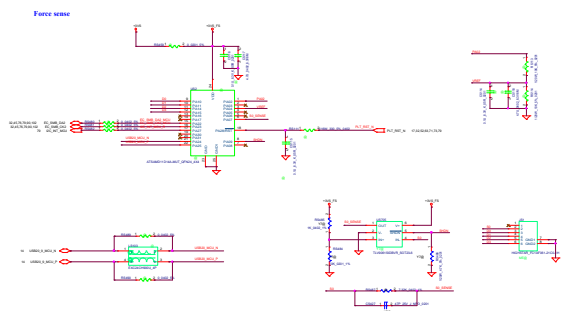


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Doc ID		Doc Number		Rev		Rev	
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Date		Issued		Rev		Rev	
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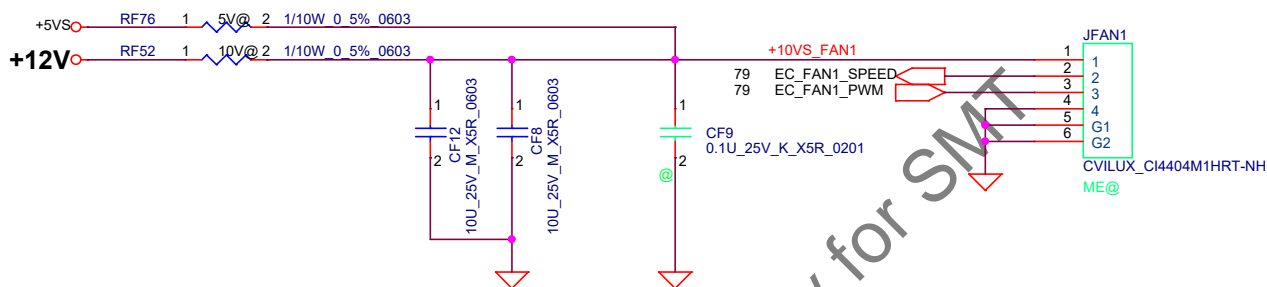
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		5		Y540	
		Date		Monday, November 18, 2021	
		Sheet		75 of 110	



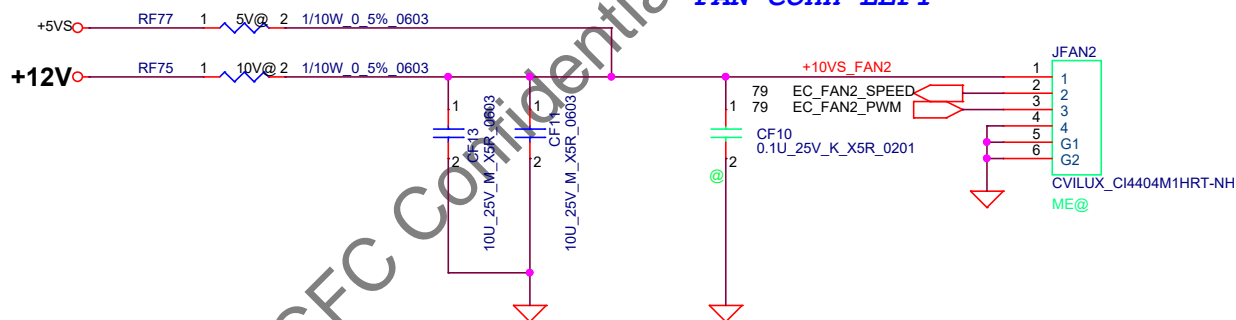
Remove TOF senser

FAN Conn Right



22U 电容换成两颗10U 0603 电容 TOP 和BOT各放一颗增加5VS 供电

FAN Conn LEFT



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Title

Thermal sensor/FAN CONN

LCFC

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2020/02/24

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Document Number

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Rev

A0

Date:

Monday, November 29, 2021

Sheet

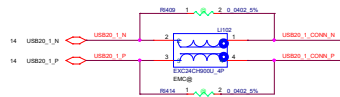
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of

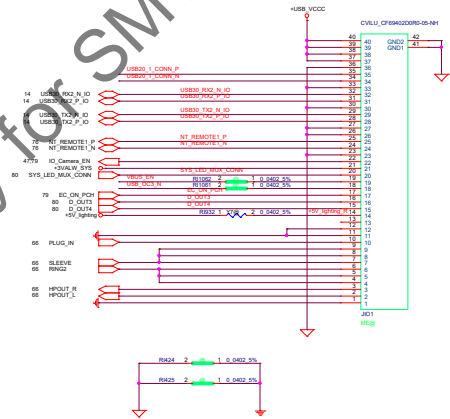
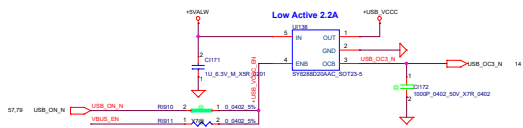
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Right Side USB2.0 Port X 1 (USB/B)

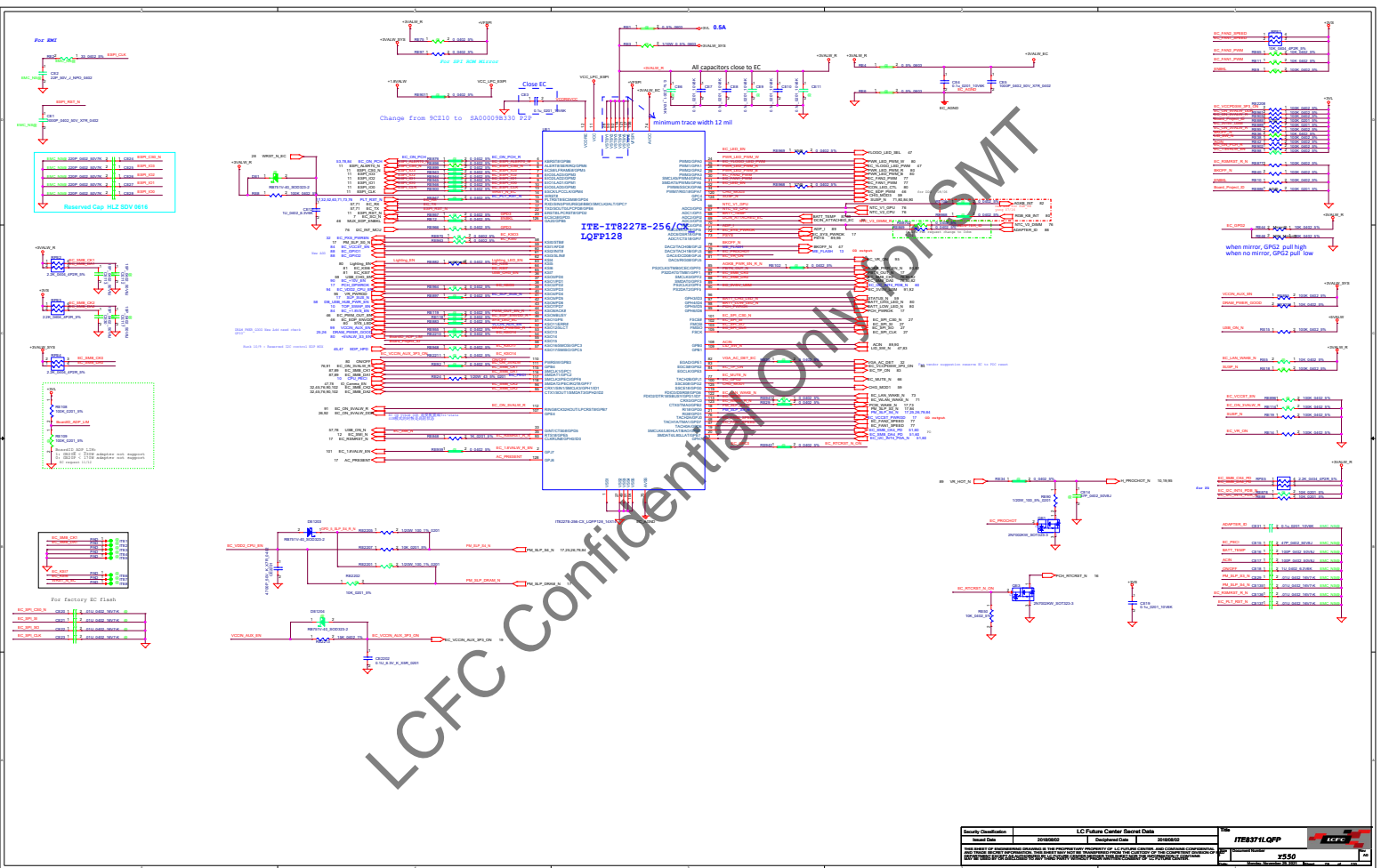


USB3.1 PORT x1

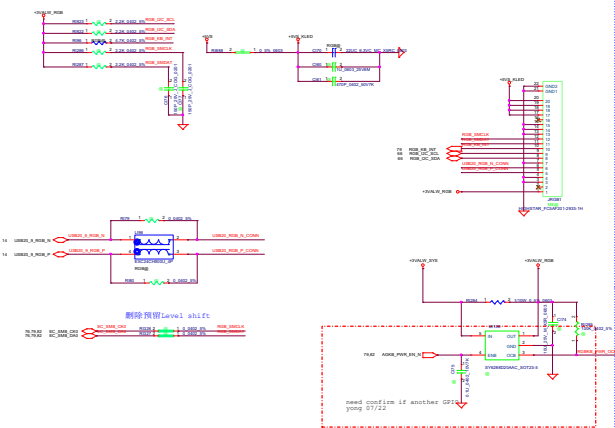


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Module Number: 26, 2021		118		Date	

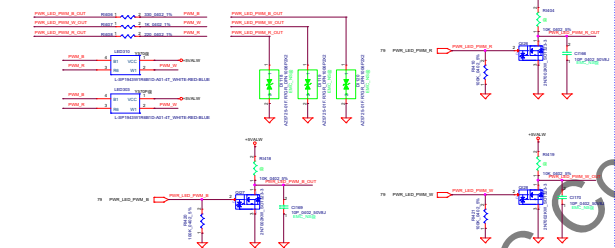
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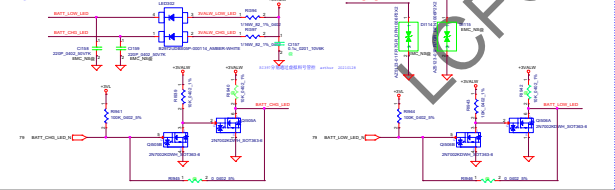
for Y560 KB lighting



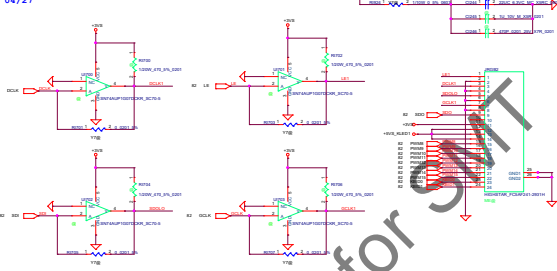
Power Button LED



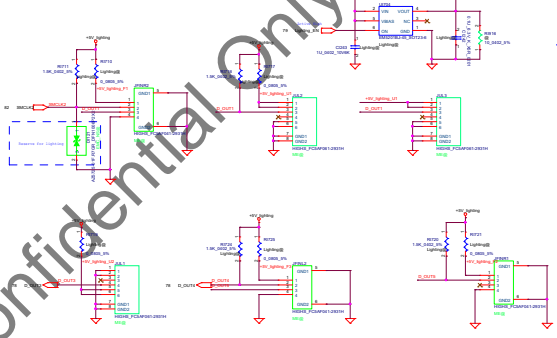
Charger LED



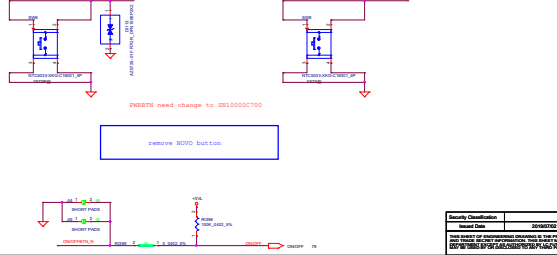
for Y760 KB lighting



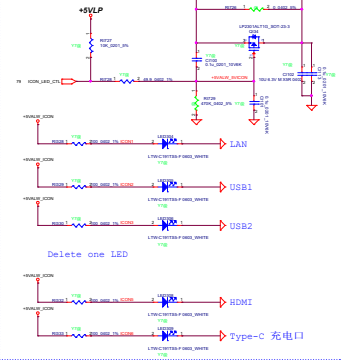
for Y760 system lighting



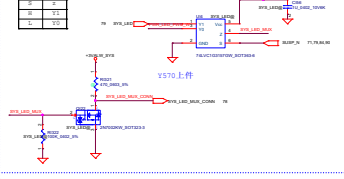
ON/OFF switch



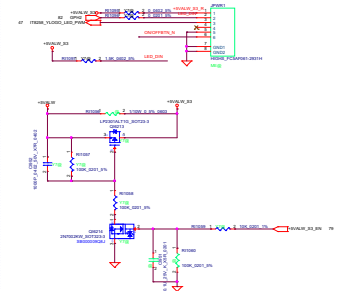
for rear side ICON LED

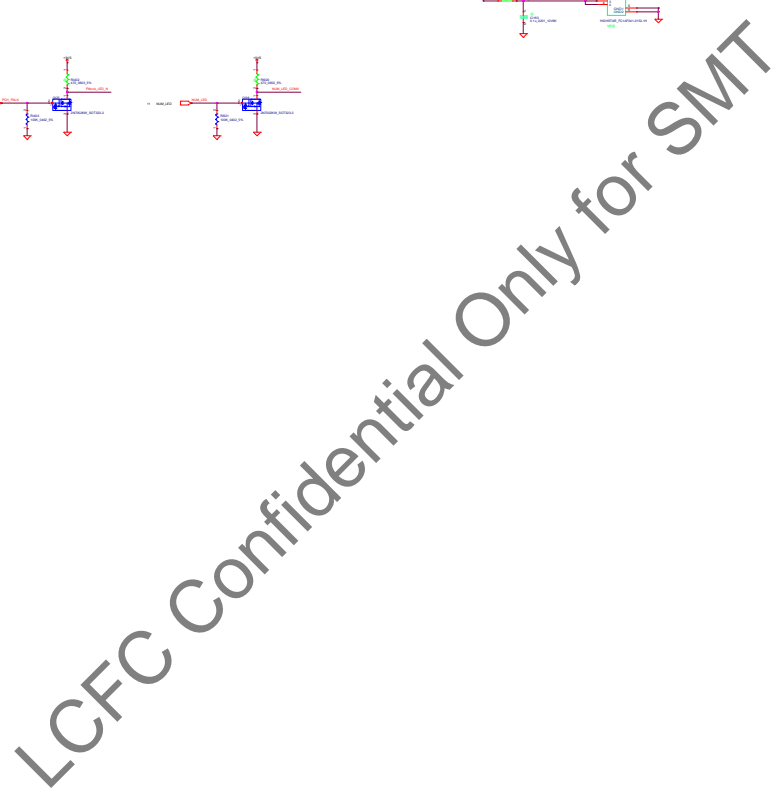


system LED

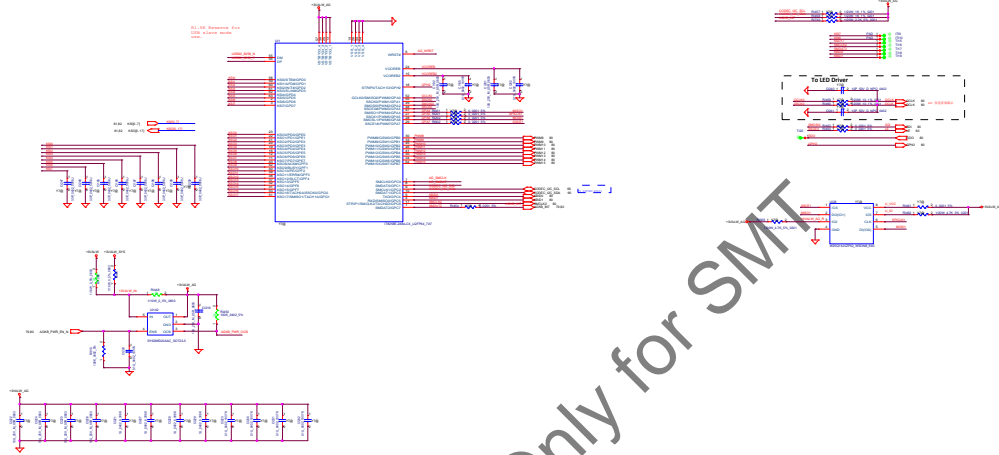


Power button for Y770

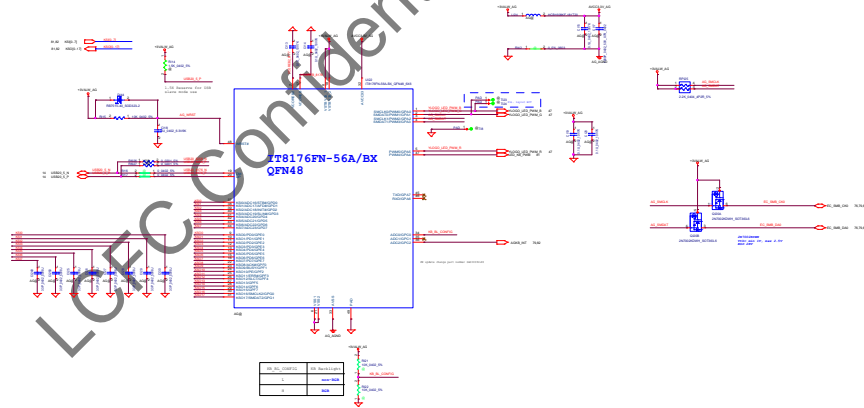


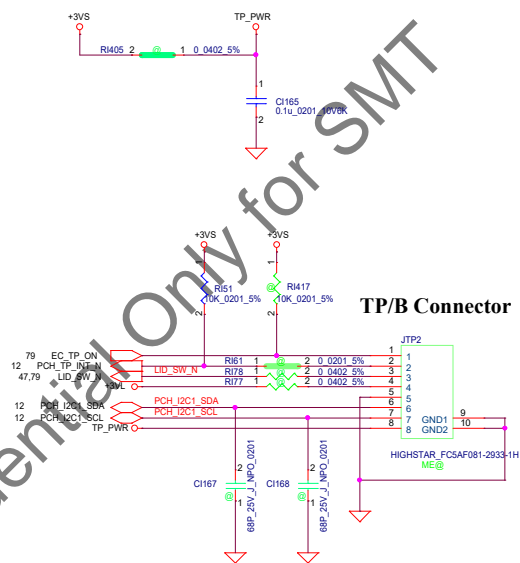
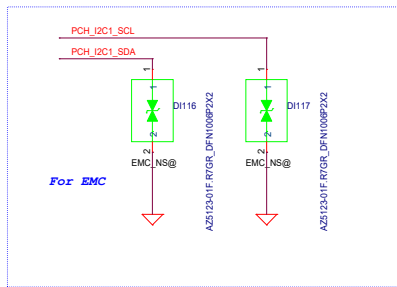


IT8258



IT8176

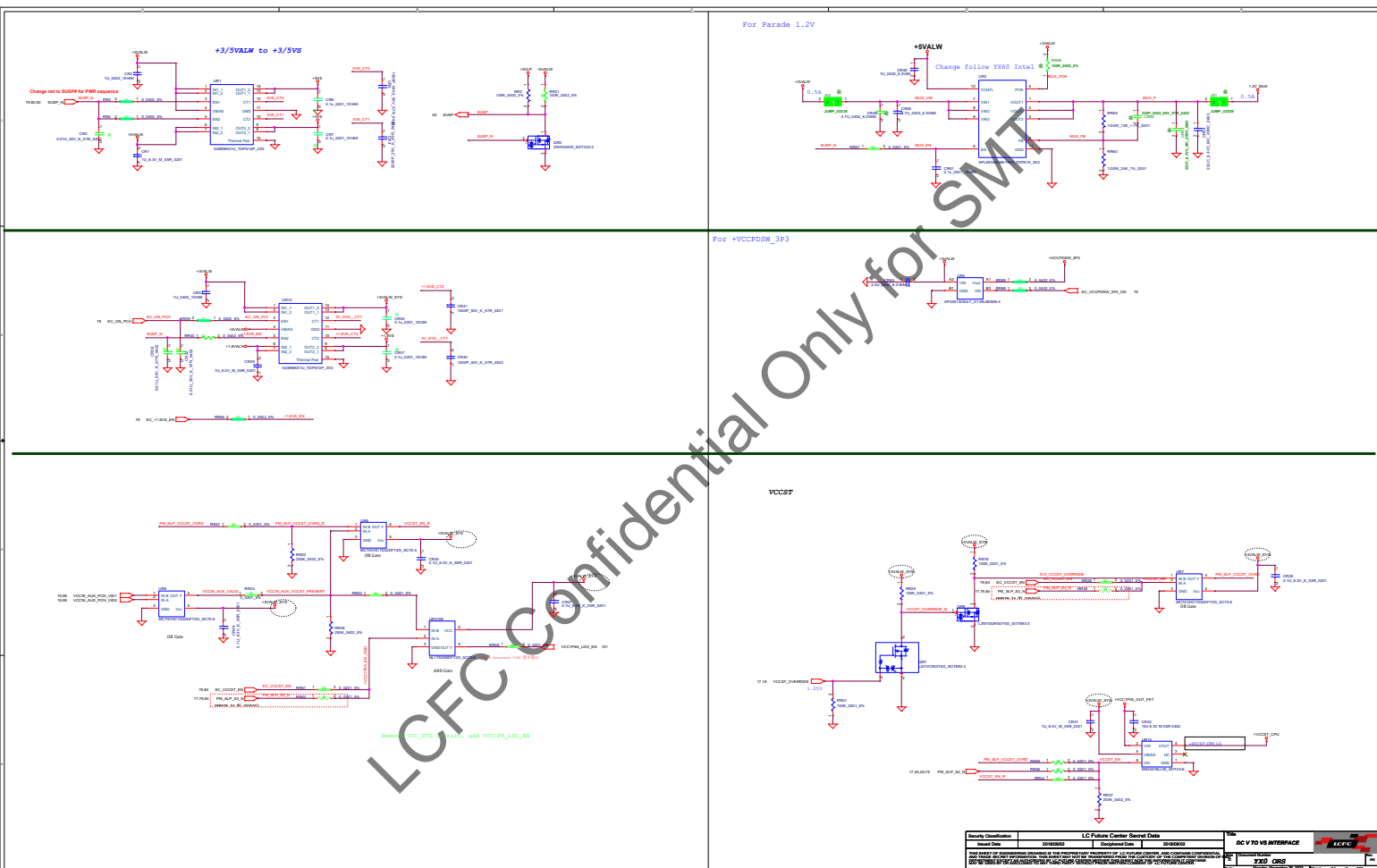





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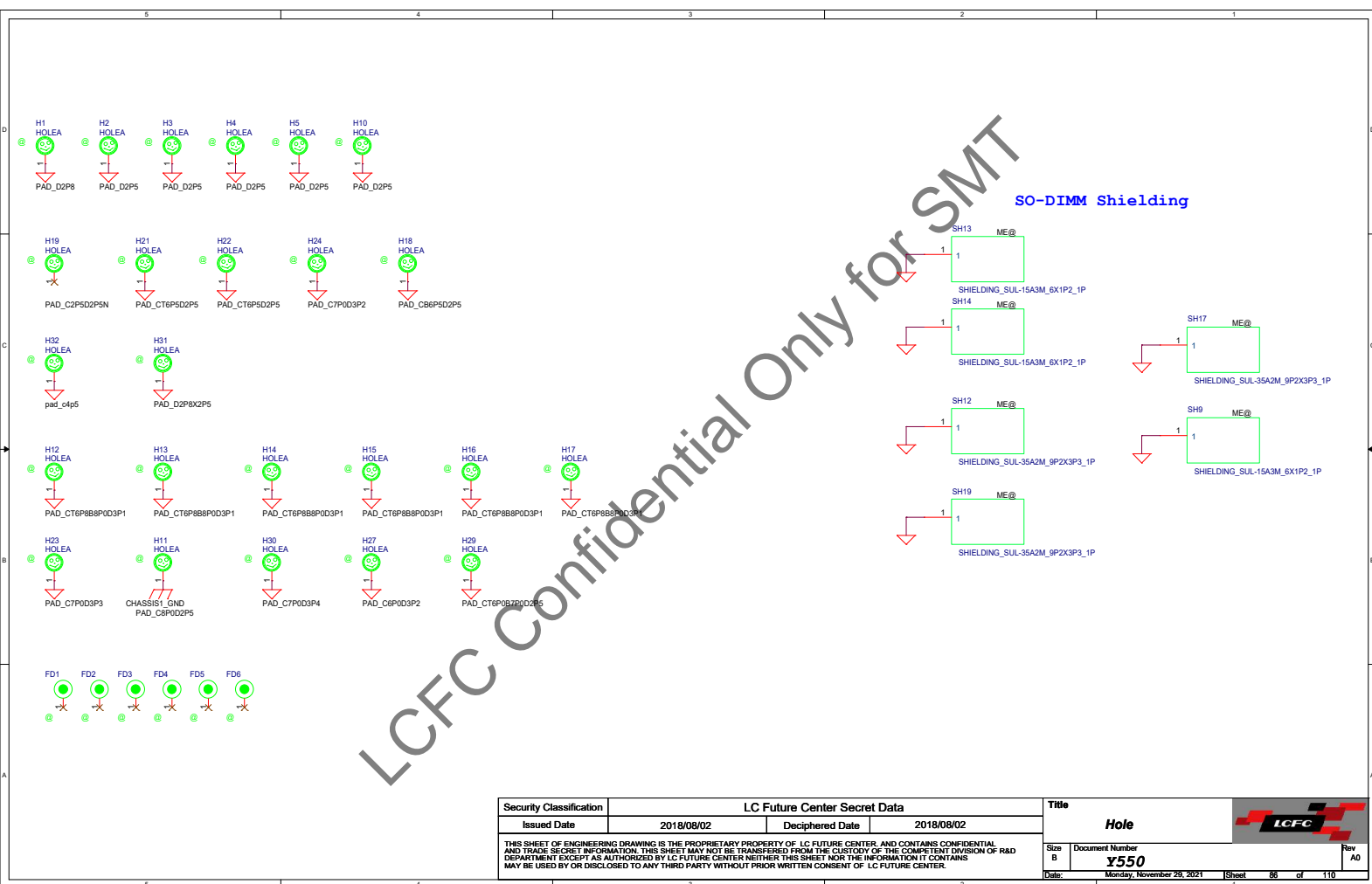
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Size	Document Number		
B	Y550	A0	



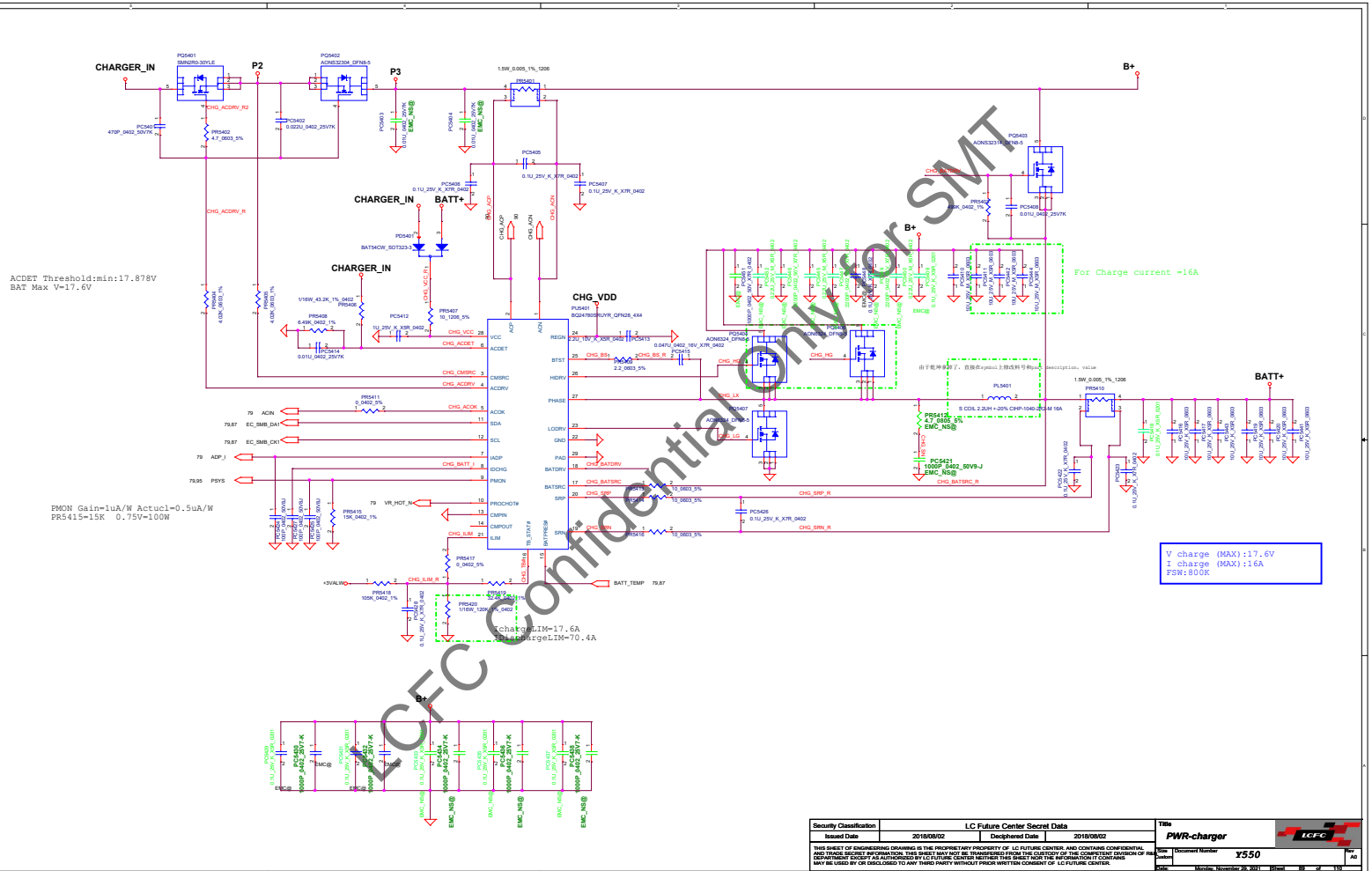
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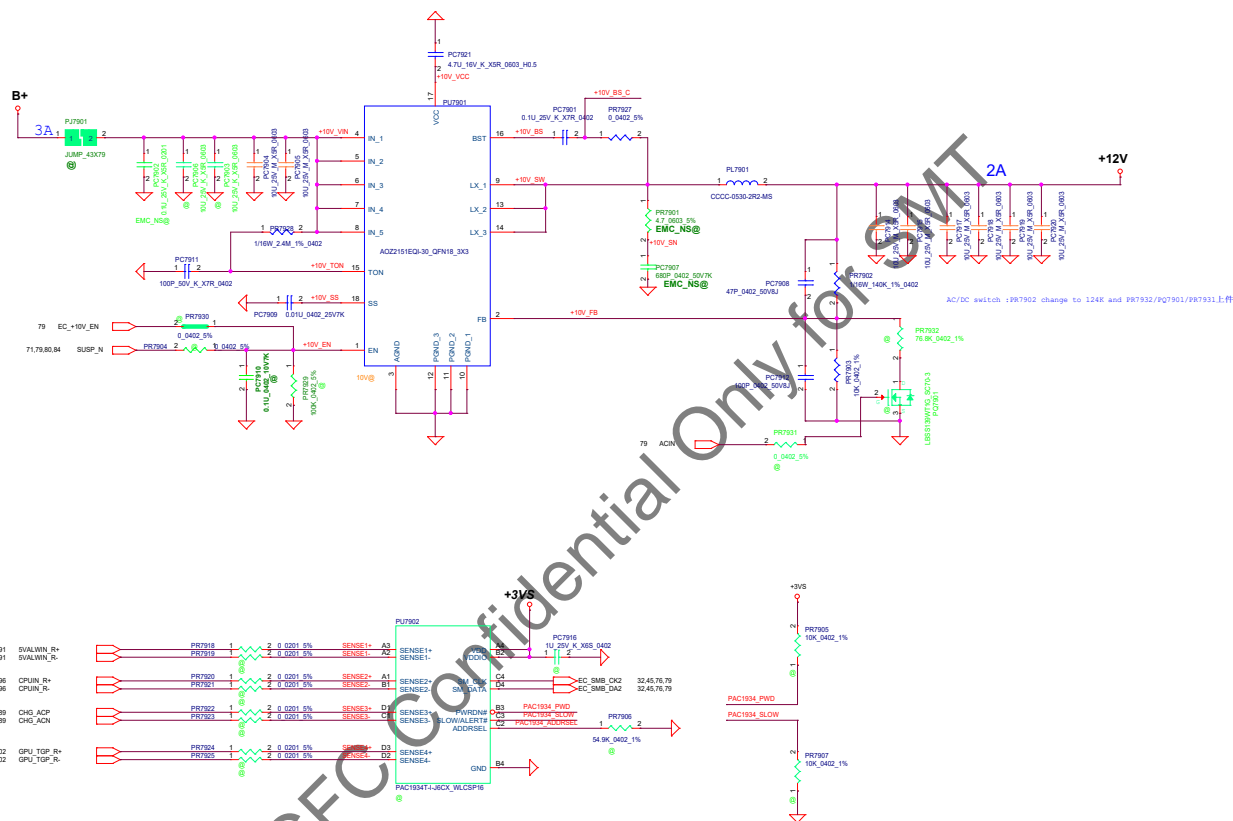
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				8	Reserved	AD
				Date:	Monday, November 26, 2021	Sheet 85 of 110



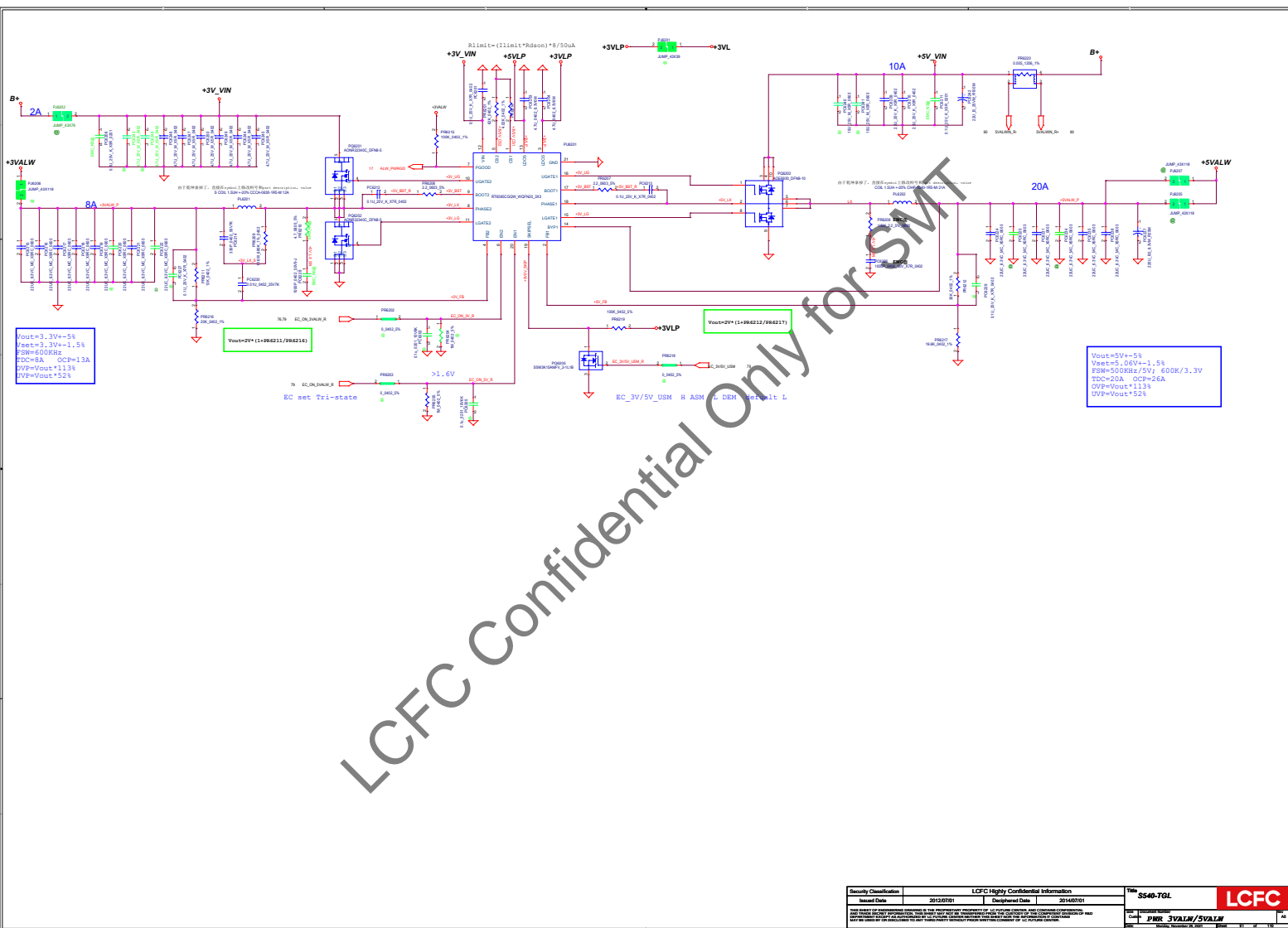
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BAT Max V=17.6V

PMON Gain=1uA/W Actuel=0.5uA/W
PR5415=15K 0.75V=100W





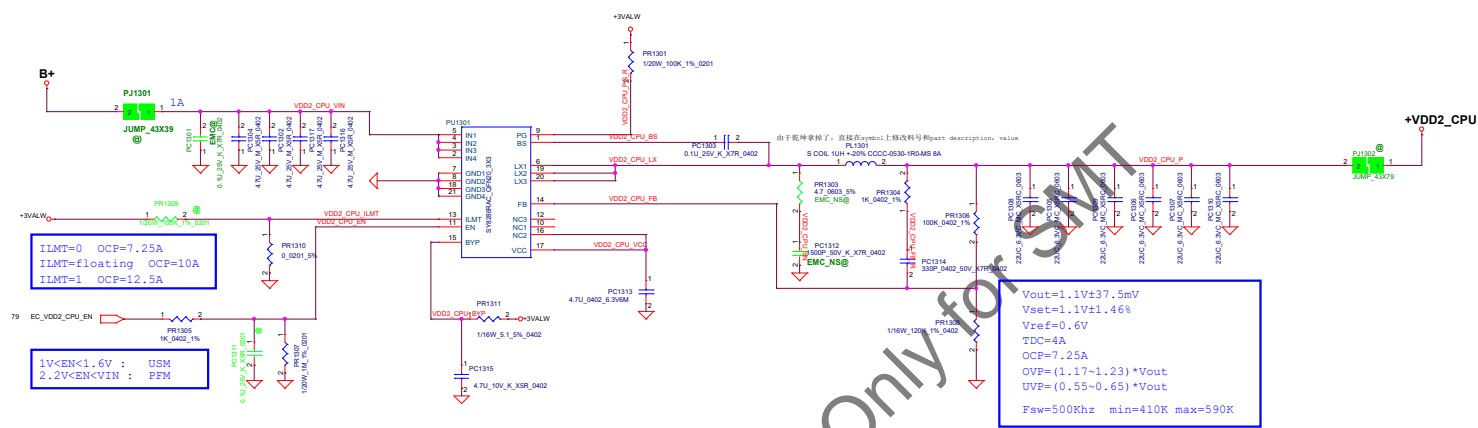
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Issued Date	2018/08/02	Declassified Date	2018/08/02	PWR_Memory PWR Decoupling	
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Size	Count	Document Number	Y360 AMD		
Date	Version	Revision	2021	10/2021	10/2021




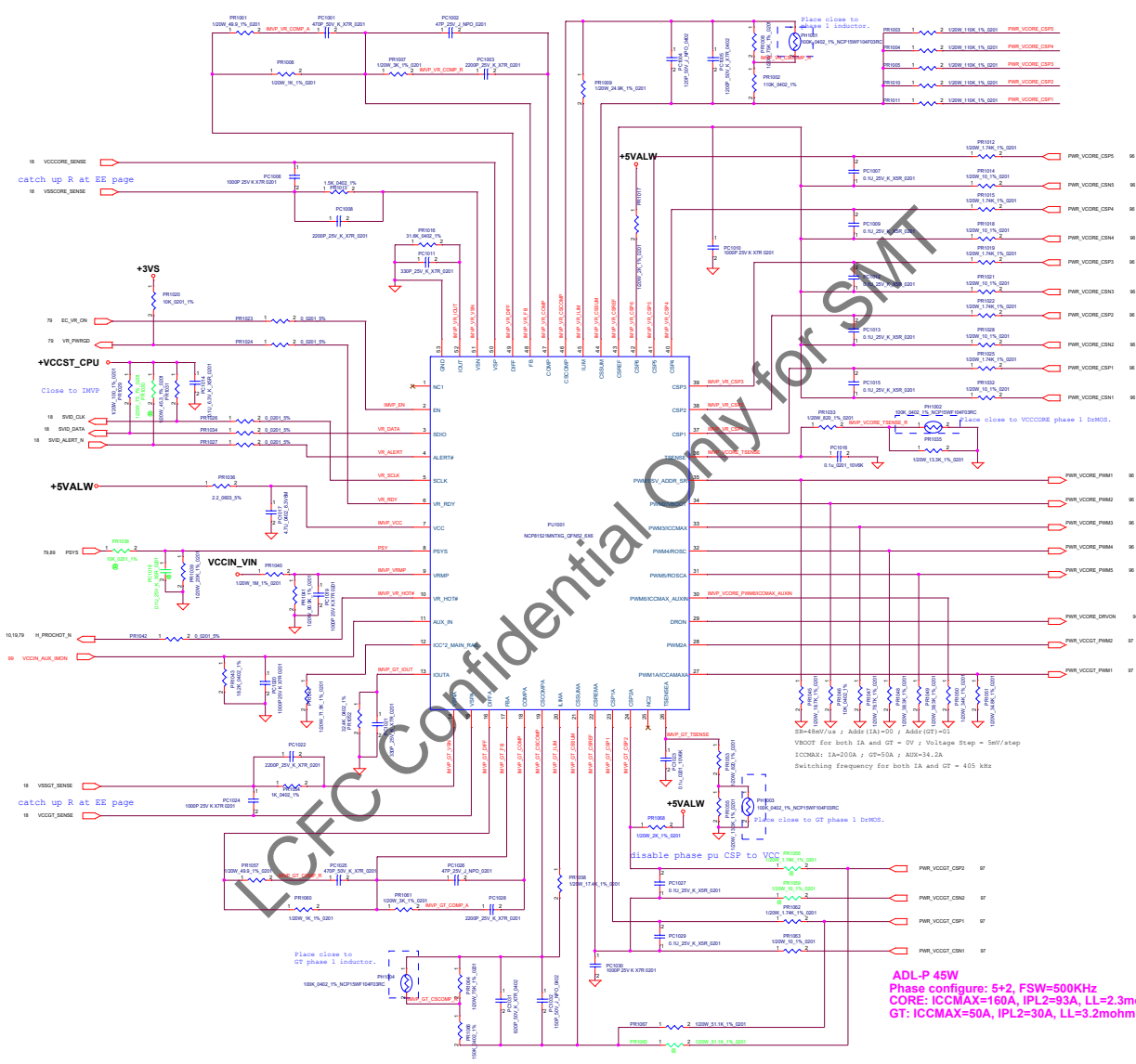
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				Y560 AMD	
				Monday, November 26, 2019 9:54 AM	

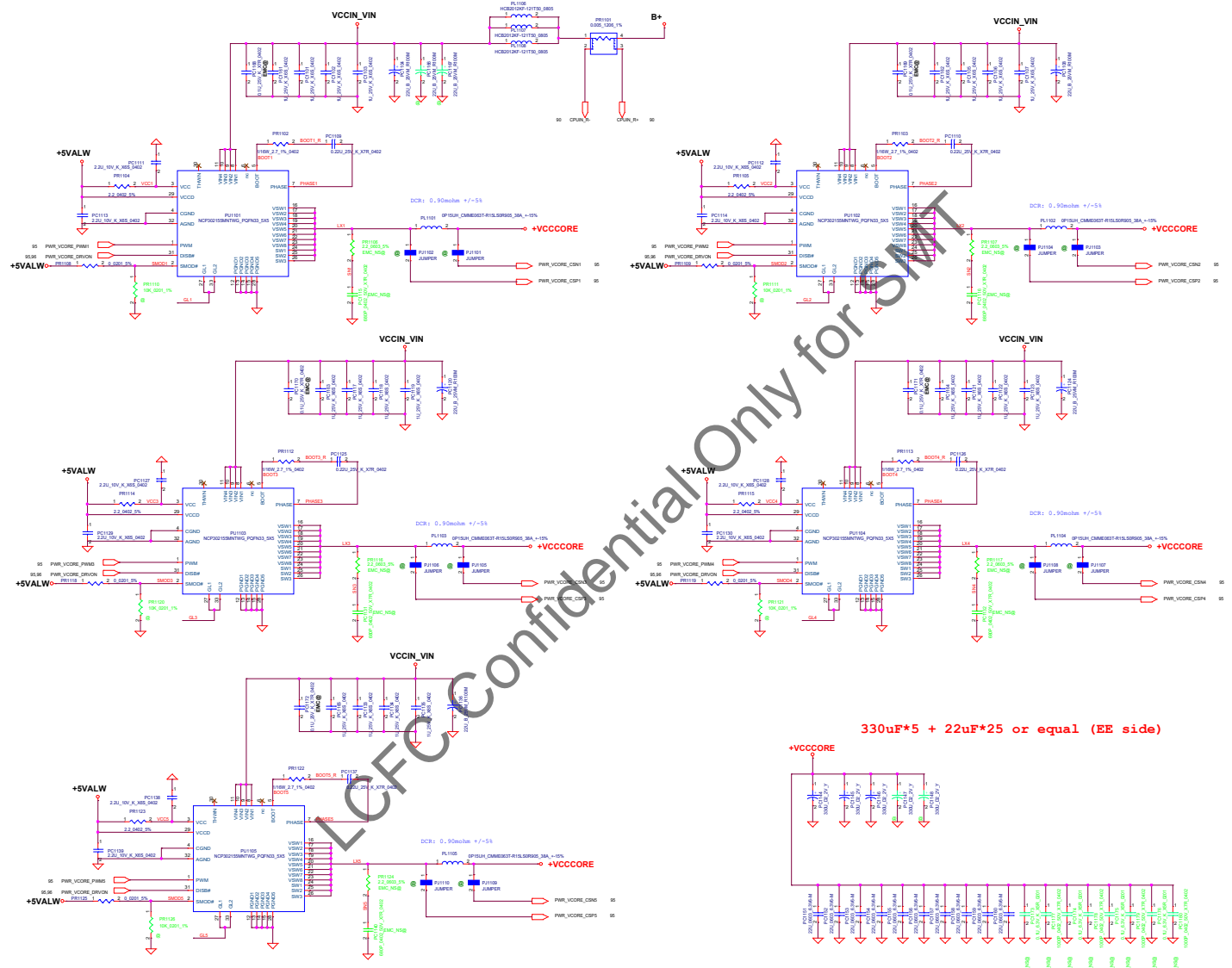
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C		Y560 AMD					1.0	
Date		Monday, November 26, 2021			Sheet		94 of 110	

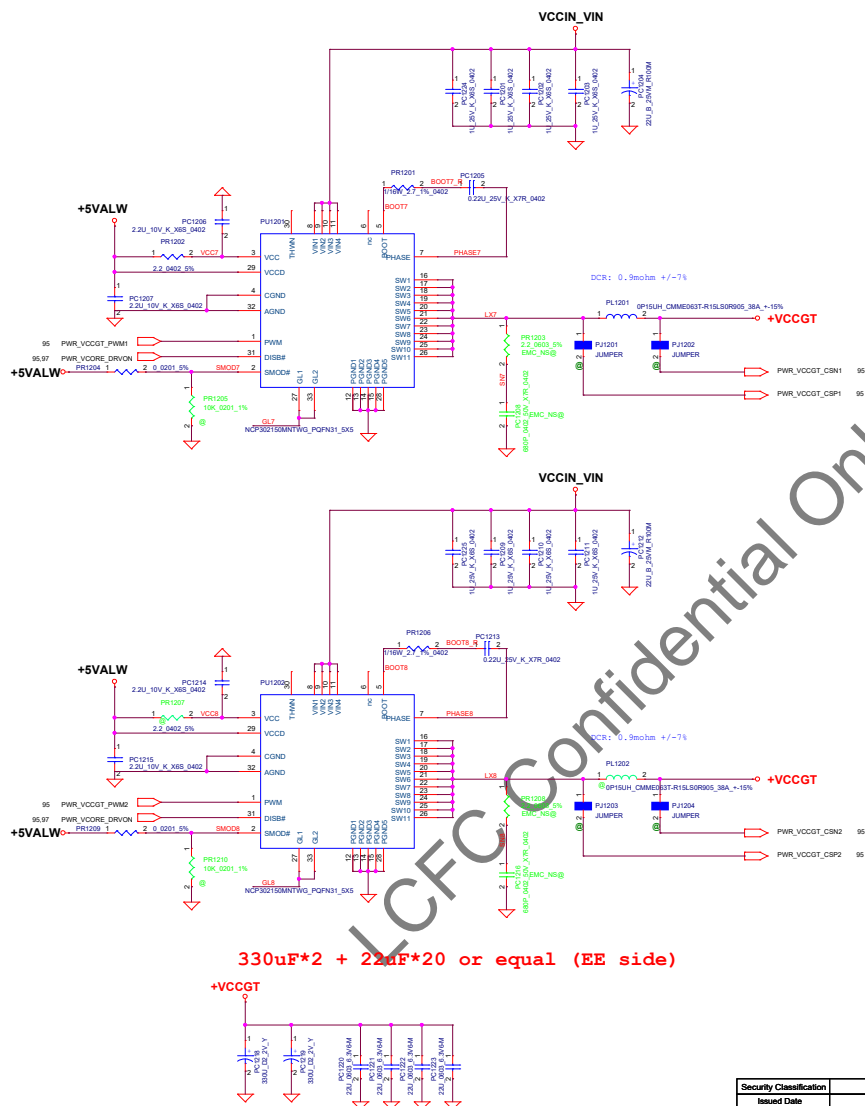



ADL-P 45W
Phase configure: 5+2, FSW=500KHz
CORE: ICCMAX=160A, IPL2=93A, LL=2.3mohm
GT: ICCMAX=50A, IPL2=30A, LL=3.2mohm



330uF*5 + 22uF*25 or equal (EE side)

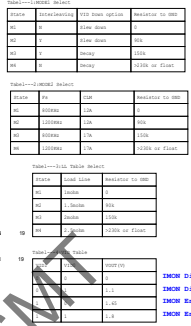
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Issued Date	20180802	Designed Date	20180802
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Doc No	Y560_AMD	Rev	1.0
Doc Name	Power Management IC	Rev	1.0




Security Classification			LC Future Center Secret Data			Title		
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Rev		Document Number		Y560 AMD		Rev		
C		Y560 AMD		Rev		1 of 114		
Date		2018/08/02		Rev		1 of 114		

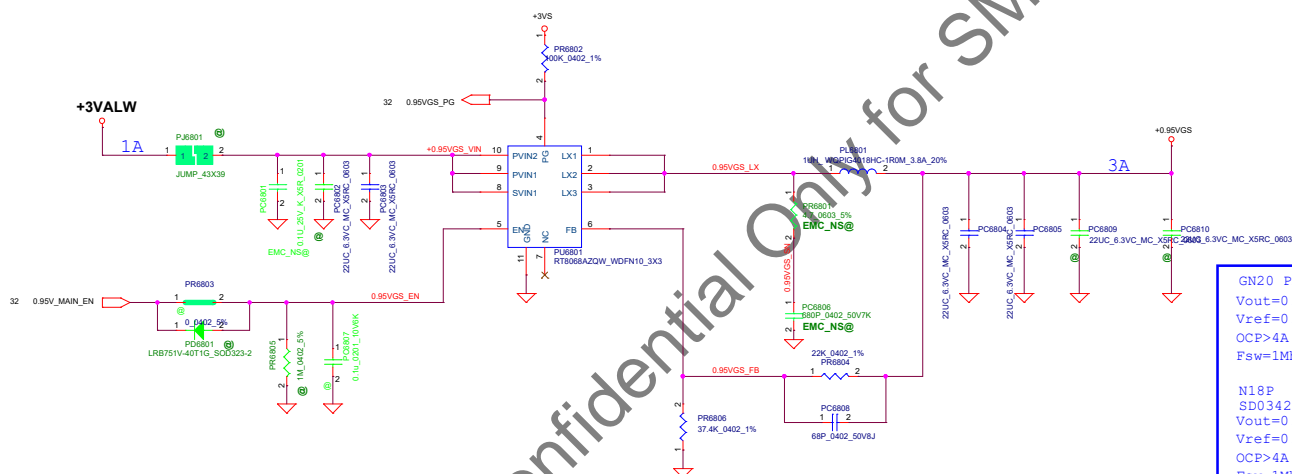
VER1.10

Model2: 800K, 19.5A/phase
Model: Non-Interleaving, Decay



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				C	Y540
				Rev	AD
Date				Monday, November 26, 2021	Sheet 100 of 119




GN20 PR6804=22K
 Vout=0.953V±3%
 Vref=0.6V
 OCP>4A
 Fsw=1Mhz


N18P PR6804=26.1K
 SD03426128J
 Vout=0.953V±3%
 Vref=0.6V
 OCP>4A
 Fsw=1Mhz

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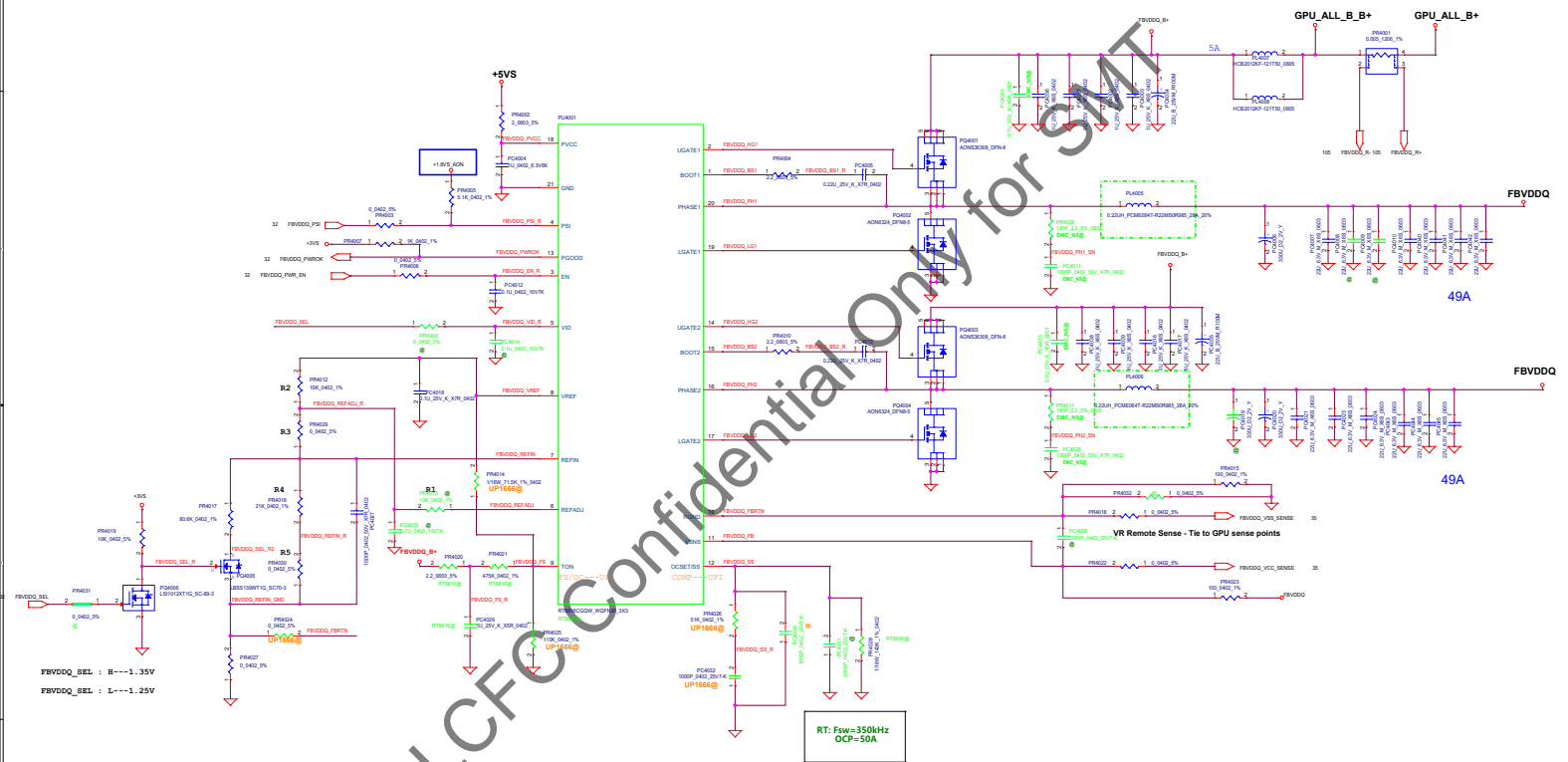
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RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.3V	1.6~5.3V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM




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				Date	Revision	Sheet
					110	110